Announcements

- Homework #8 due next Tuesday

- Project Phase 3 part 1 due this Sun.
  - Poster: Wed. Nov. 28th
  - Final report: Mon. Dec. 3rd

- This Thurs. lecture will be “taped ahead”
Sequential Elements: Flops and Latches

Why Sequencing?
Sequential Elements

- **Latch** – level sensitive
  - Clk=0: “opaque”
  - Clk-1: “transparent”

- **Flip-flop** – edge triggered
  - Stores new data when Clk rises

Timing Definitions - REVIEW

- Register
  - **D**
  - **Q**

- DATA STABLE
  - **t**
  - **t_{su}**
  - **t_{final}**
  - **t_{delay}**

- DATA STABLE
  - **t**
Storage Mechanisms

Dynamic Latch

Static Latch

Writing Into a Static Latch

Forcing the state

Converting into a MUX (gated feedback)
Master-Slave Flip-Flop (Edge-Triggered Register)

Two opposite latches create edge-triggered behavior
Also called master-slave latch pair

Master-Slave Register

Multiplexer-based latch pair
Register Timing: Clk-Q Delay

- $t_{clk-q(LH)}$
- $t_{clk-q(HL)}$

Volts vs. time, nsec

Register Timing: Setup Time

(a) $T_{setup} = 0.21$ nsec
(b) $T_{setup} = 0.20$ nsec
More Precise Setup Time

Setup-Hold Time Illustrations
**Setup-Hold Time Illustrations**

Circuit before clock arrival (Setup-1 case)

- **Data**
- **Clock**
- **Circuit before clock arrival (Setup-1 case)**

- **Inv1**
- **Inv2**
- **TG1**
- **CP**
- **D**
- **Q_M**
- **S_M**

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

- **Data**
- **Clock**
- **Circuit before clock arrival (Setup-1 case)**

- **Inv1**
- **Inv2**
- **TG1**
- **CP**
- **D**
- **Q_M**
- **S_M**

EECS141 Lecture #23
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data

Clock

Time

t=0

Clk-Q Delay

T_{Setup-1}

T_{Clk-Q}

T_{Hold-1}

D

Inv1

CN

TG1

D1

S_M

Inv2

Q_M

CP

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data

Clock

Time

t=0

Clk-Q Delay

T_{Setup-1}

T_{Clk-Q}

T_{Hold-1}
Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case
Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

D

Inv1

TG1

D{

Inv2

S_M

Q_M

Clk-Q Delay

THold-1

TClk-Q

0

Time

Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

D

Inv1

TG1

Inv2

S_M

Q_M

Clk-Q Delay

THold-1

TClk-Q

Time
**Setup-Hold Time Illustrations**

*Hold-1 case*

![Diagram of Clk-Q Delay and setup-hold time with labels](image)

**Other Latches/Registers: C²MOS**

*Usually includes feedback to staticize*

![Diagram of C²MOS latches](image)
C^2MOS and Clock Overlap

Other Latches/Registers: TSPC

Positive latch (transparent when CLK= 1)  Negative latch (transparent when CLK= 0)
**TSPC Operation**

![TSPC Circuit Diagram]

**Other Latches/Registers: Pulse-Triggered Latches**

- Master-Slave Latches
- Pulse-Triggered Latch
Why not route the pulse?

Next Lecture

- Timing