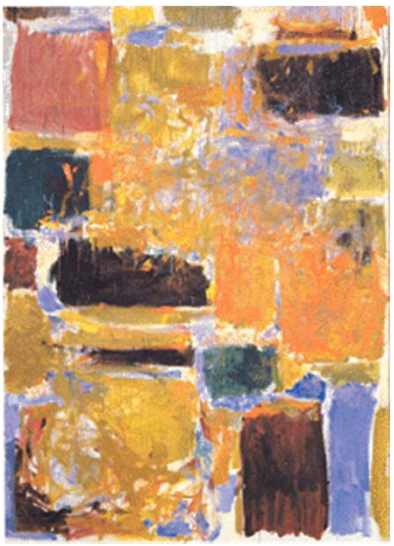


EE141-Fall 2012 Digital Integrated Circuits

Lecture 23
Flops and Latches

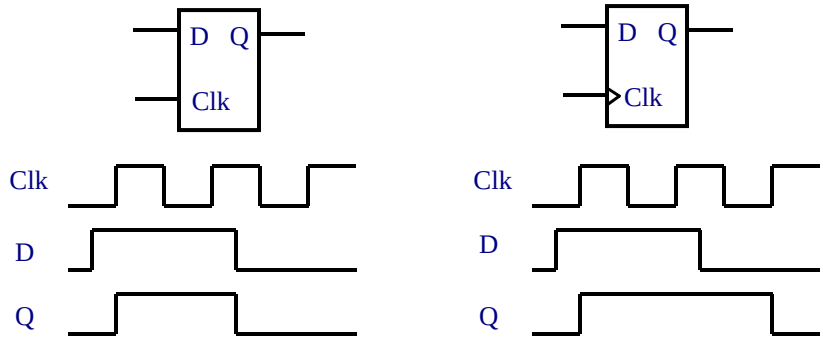
Announcements

- Homework #8 due next Tuesday
- Project Phase 3 part 1 due this Sun.
  - Poster: Wed. Nov. 28th
  - Final report: Mon. Dec. 3rd
- This Thurs. lecture will be "taped ahead"

Sequential Elements: Flops and Latches

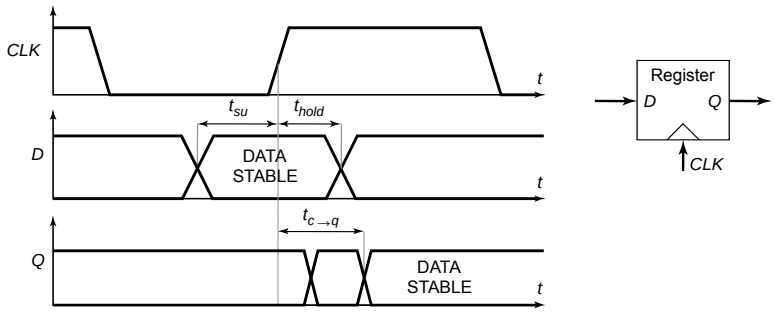
Why Sequencing?

Sequential Elements

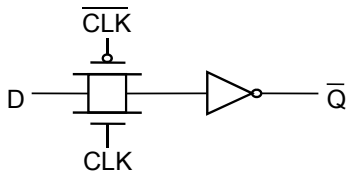


- Latch – level sensitive
  - Clk=0: “opaque”
  - Clk-1: “transparent”
- Flip-flop – edge triggered
  - Stores new data when Clk rises

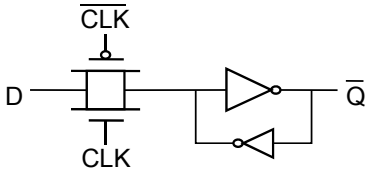
Timing Definitions - REVIEW



Storage Mechanisms

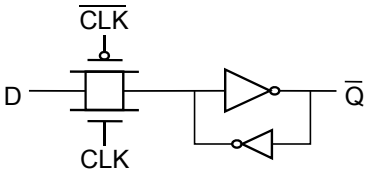


Dynamic Latch

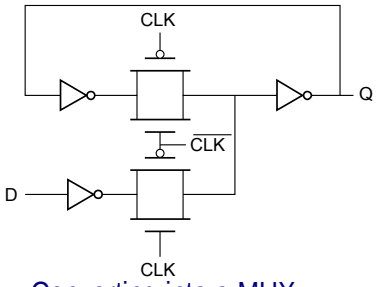


Static Latch

Writing Into a Static Latch

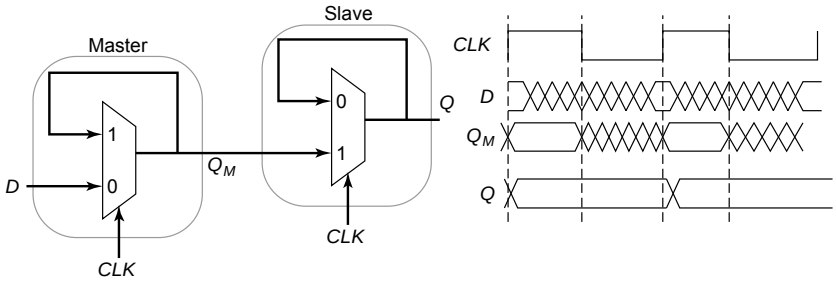


Forcing the state



Converting into a MUX
(gated feedback)

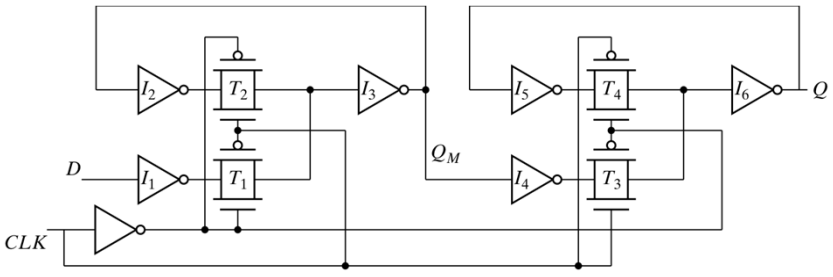
Master-Slave Flip-Flop (Edge-Triggered Register)



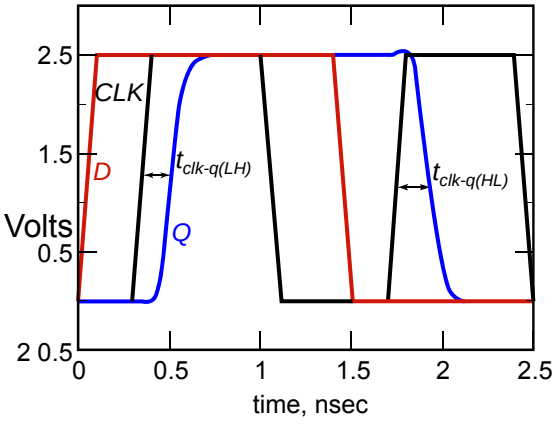
Two opposite latches create edge-triggered behavior
Also called master-slave latch pair

Master-Slave Register

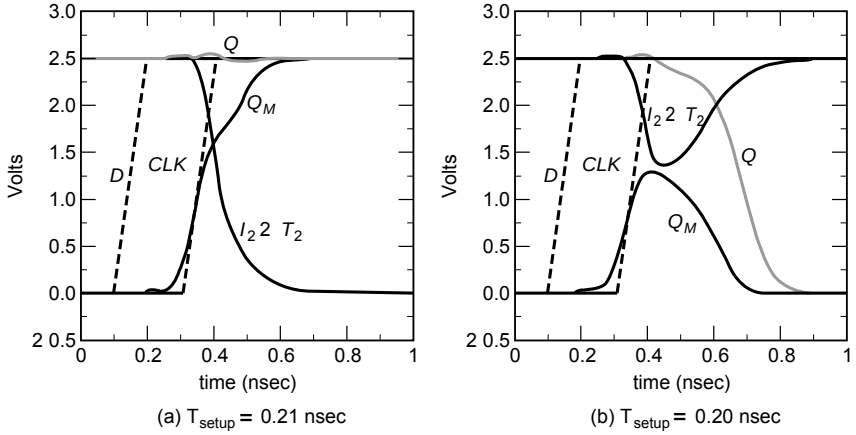
Multiplexer-based latch pair



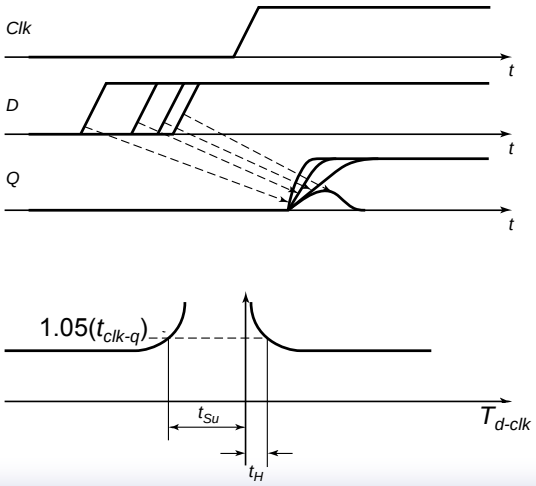
Register Timing: Clk-Q Delay



Register Timing: Setup Time

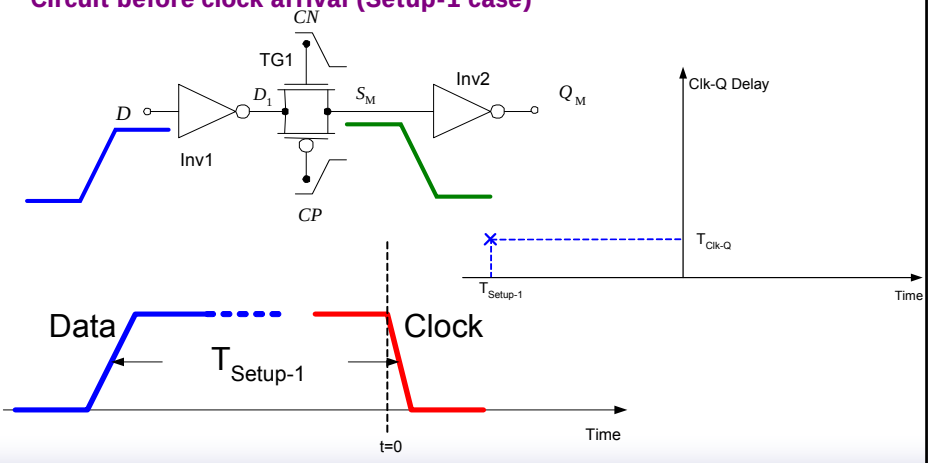


More Precise Setup Time



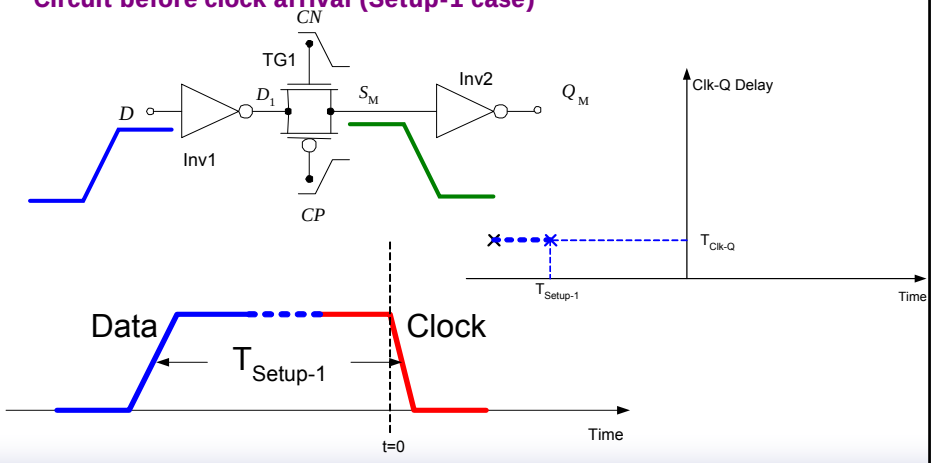
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



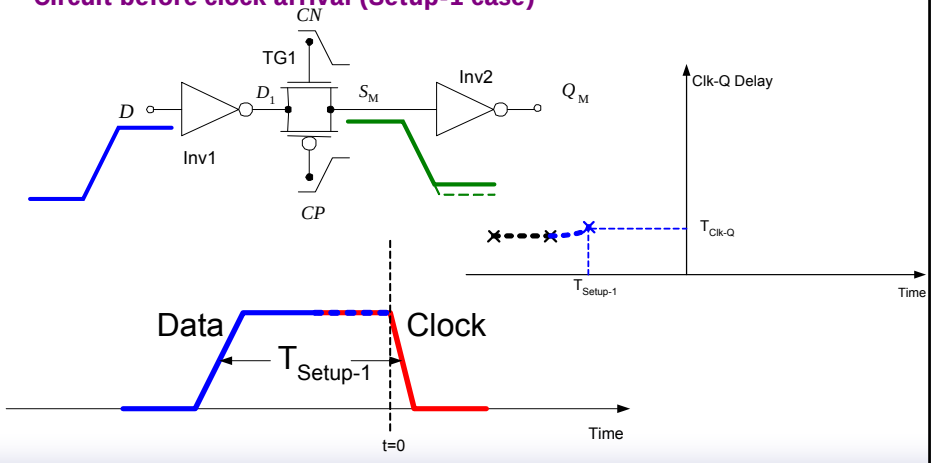
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



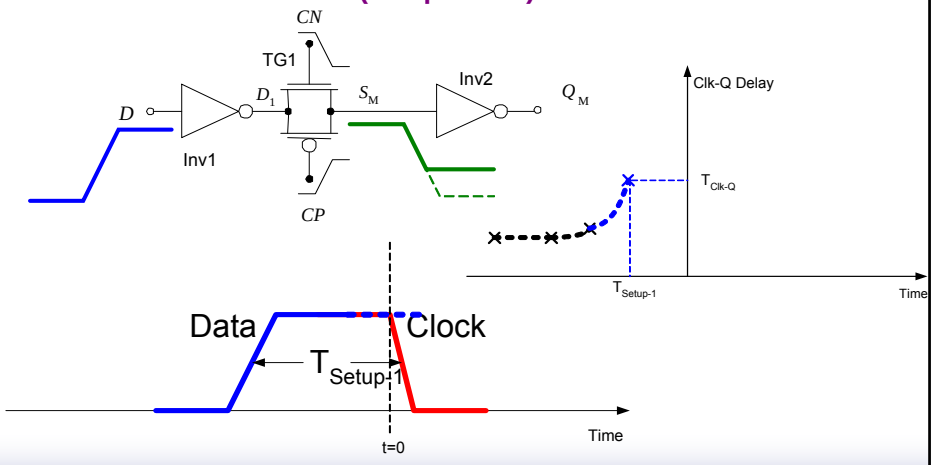
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



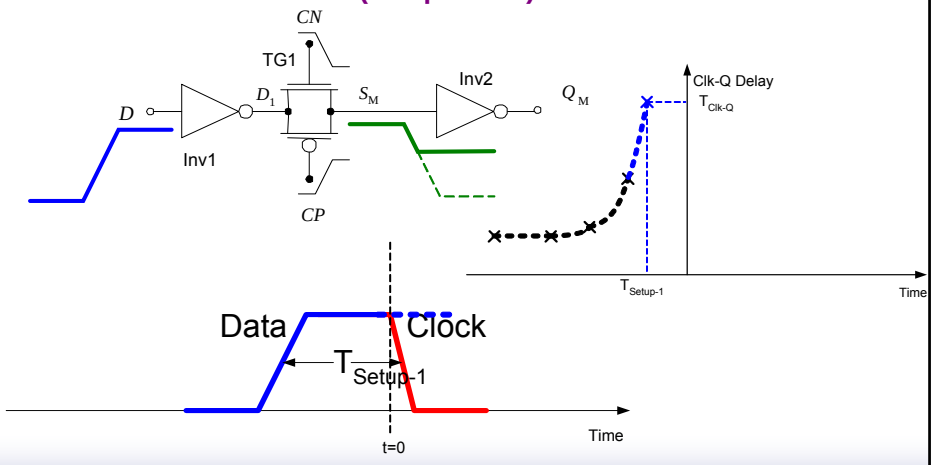
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



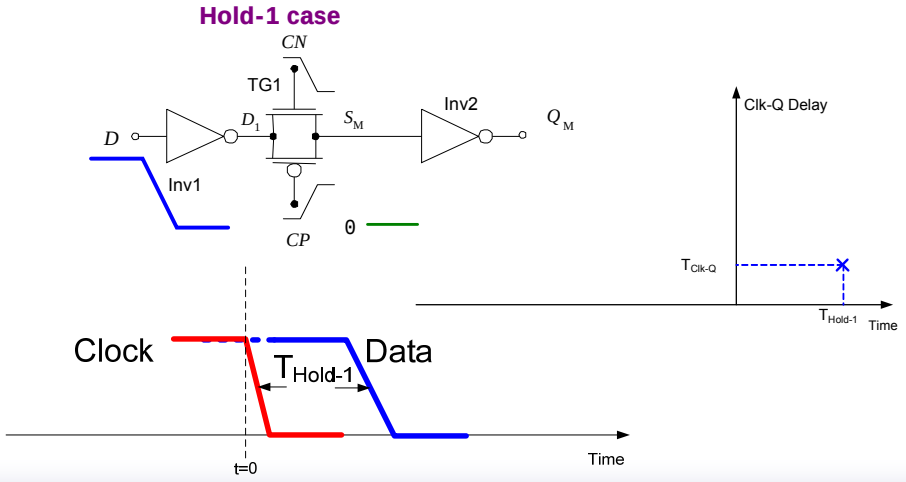
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



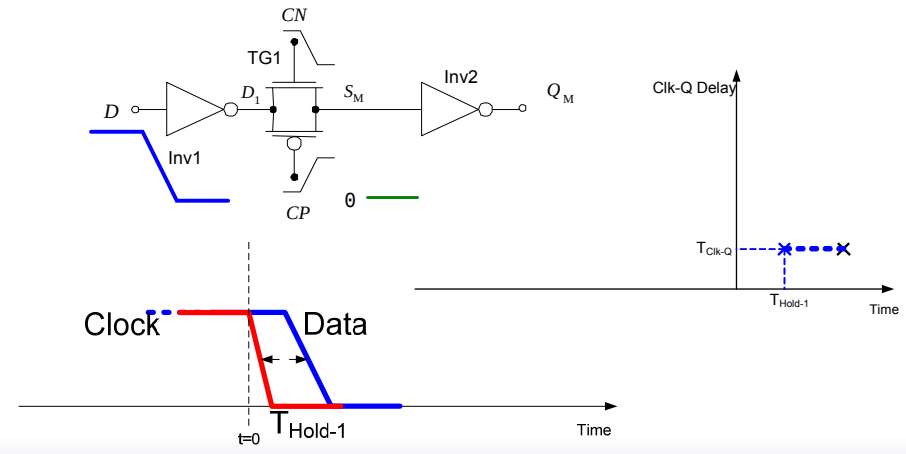
Setup-Hold Time Illustrations

Hold-1 case

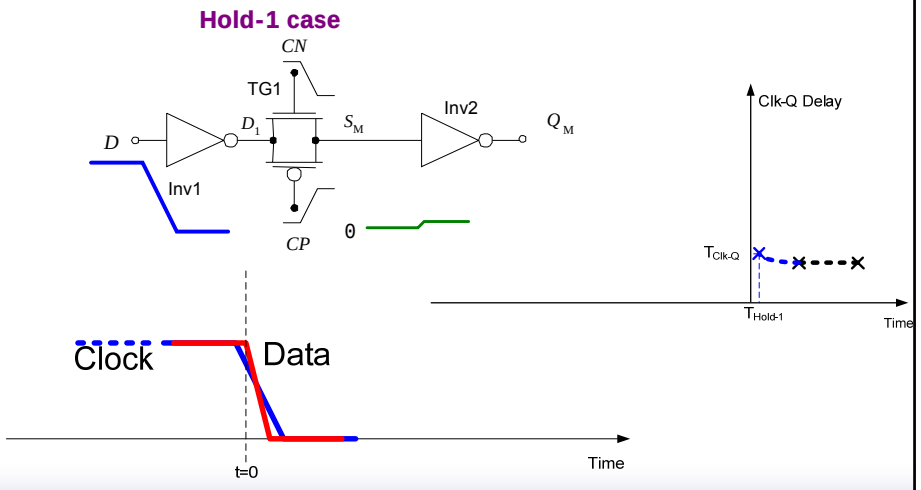


Setup-Hold Time Illustrations

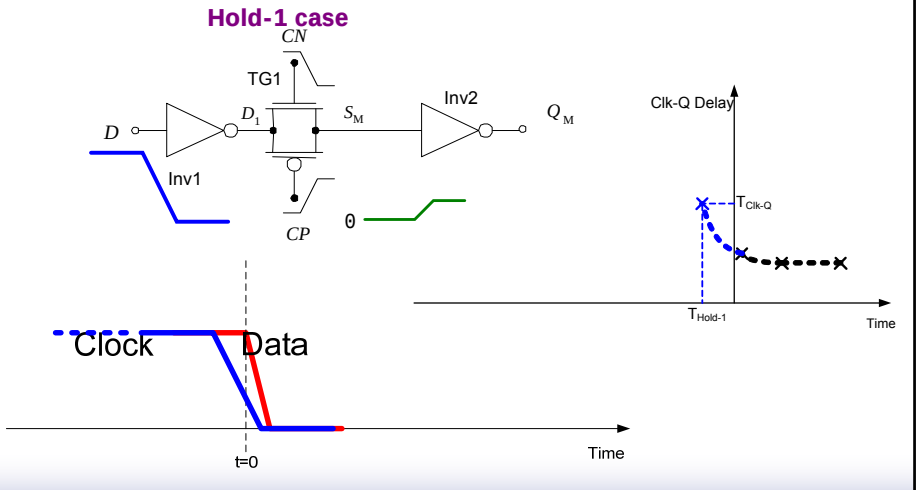
Hold-1 case



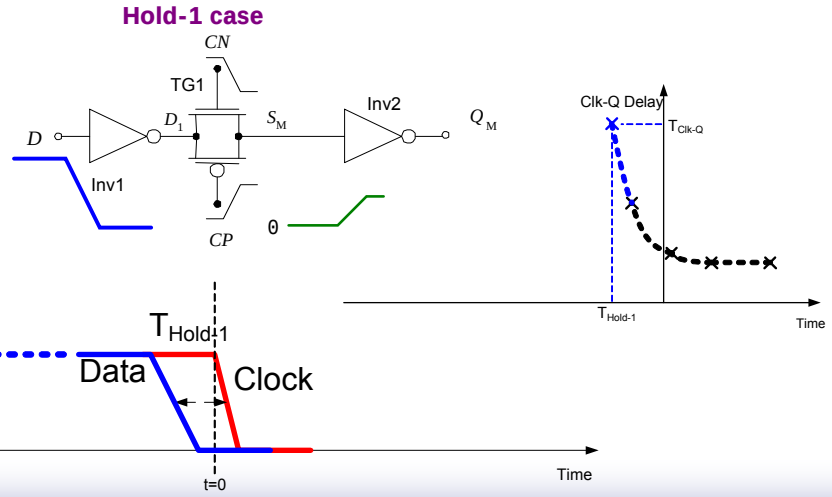
Setup-Hold Time Illustrations



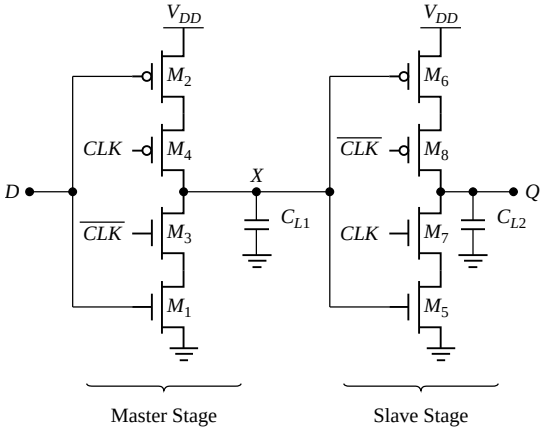
Setup-Hold Time Illustrations



Setup-Hold Time Illustrations



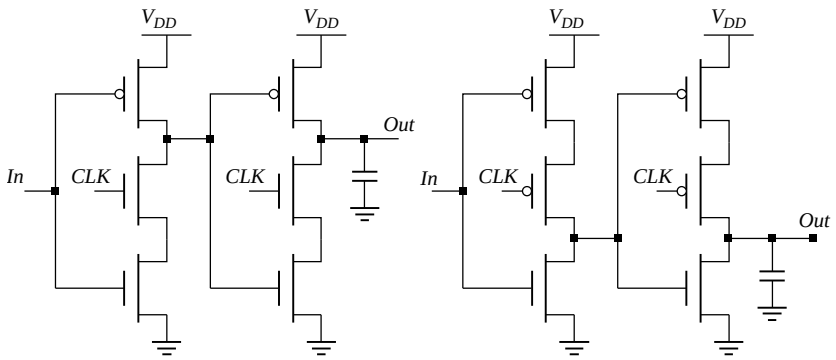
Other Latches/Registers: C²MOS



*Usually includes feedback to staticize

C^2MOS and Clock Overlap

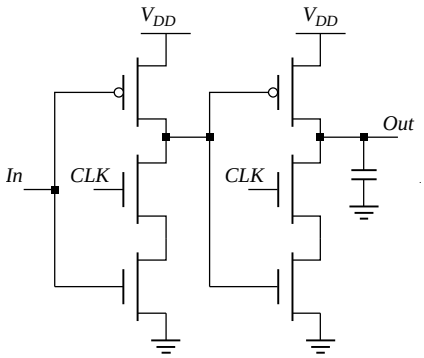
Other Latches/Registers: TSPC



Positive latch
(transparent when CLK= 1)

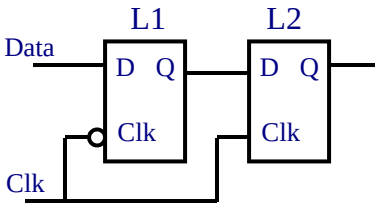
Negative latch
(transparent when CLK= 0)

TSPC Operation

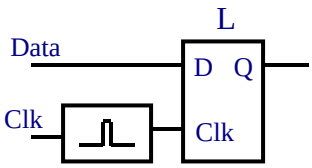


Other Latches/Registers: Pulse-Triggered Latches

Master-Slave Latches



Pulse-Triggered Latch



Why not route the pulse?

Next Lecture

- Timing