

*EE141-Fall 2012
Digital Integrated
Circuits*

Lecture 23
Flops and Latches

EECS141 Lecture #23 1

Why Sequencing?


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Announcements

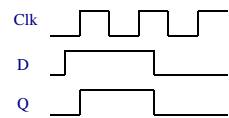
- Homework #8 due next Tuesday
- Project Phase 3 part 1 due this Sun.
 - Poster: Wed. Nov. 28th
 - Final report: Mon. Dec. 3rd
- This Thurs. lecture will be “taped ahead”


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Sequential Elements

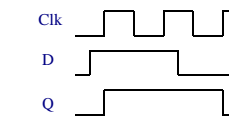


Clk






Clk



- Latch – level sensitive
 - Clk=0: “opaque”
 - Clk-1: “transparent”
- Flip-flop – edge triggered
 - Stores new data when Clk rises

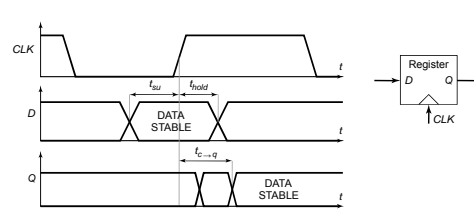
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*Sequential Elements:
Flops and Latches*

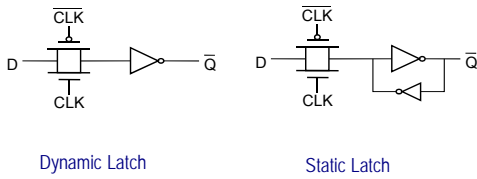
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Timing Definitions - REVIEW



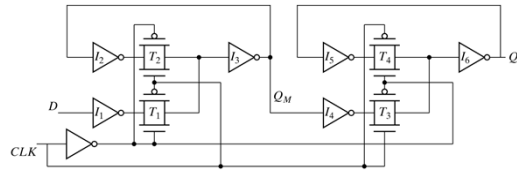
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Storage Mechanisms

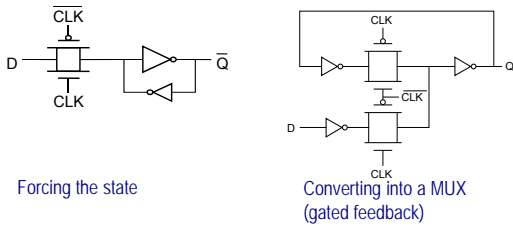


Master-Slave Register

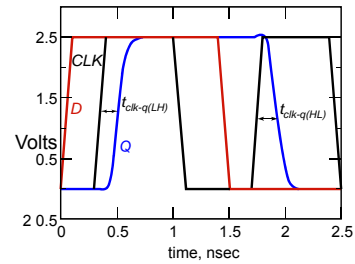
Multiplexer-based latch pair



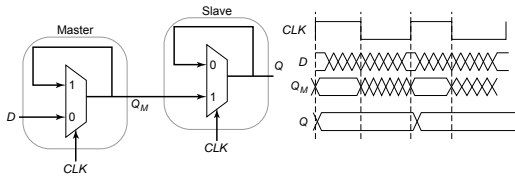
Writing Into a Static Latch



Register Timing: Clk-Q Delay

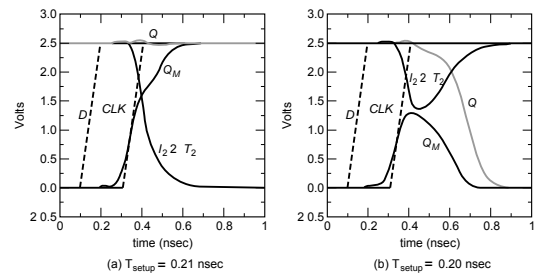


Master-Slave Flip-Flop (Edge-Triggered Register)

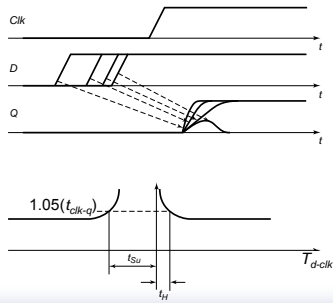


Two opposite latches create edge-triggered behavior
Also called master-slave latch pair

Register Timing: Setup Time



More Precise Setup Time



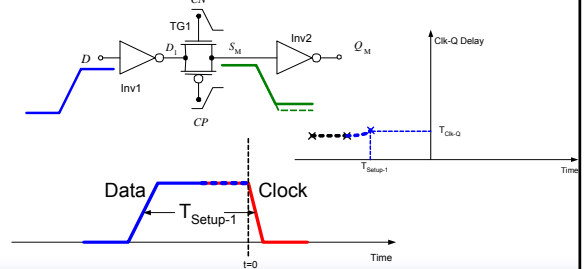
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Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



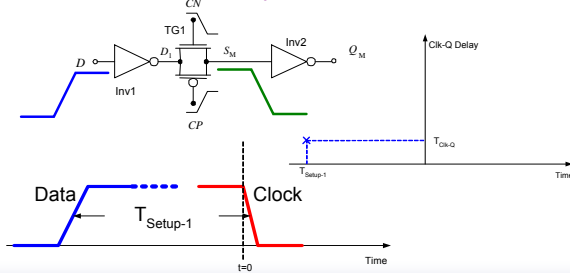
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Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



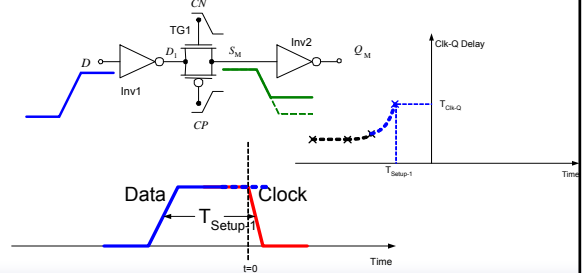
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Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



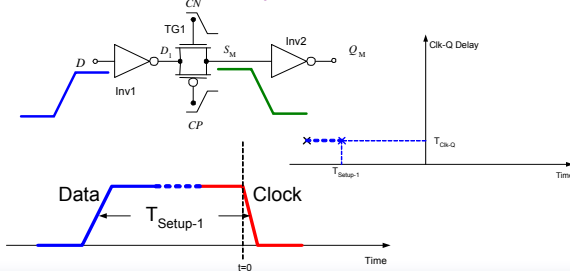
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Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



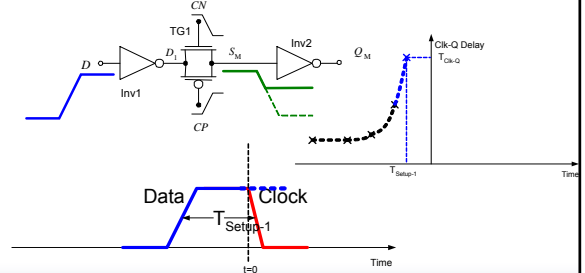
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Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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Setup-Hold Time Illustrations

Hold-1 case

Clock $t=0$ Data T_{Hold-1} Time

Clk-Q Delay T_{Clk-Q} T_{Rise-1} Time

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Setup-Hold Time Illustrations

Hold-1 case

Clock $t=0$ Data T_{Hold-1} Time

Clk-Q Delay T_{Clk-Q} T_{Rise-1} Time

EECS141 Lecture #23 22

Setup-Hold Time Illustrations

Hold-1 case

Clock $t=0$ Data T_{Hold-1} Time

Clk-Q Delay T_{Clk-Q} T_{Rise-1} Time

EECS141 Lecture #23 20

Setup-Hold Time Illustrations

Hold-1 case

Clock $t=0$ Data T_{Hold-1} Time

Clk-Q Delay T_{Clk-Q} T_{Rise-1} Time

EECS141 Lecture #23 23

Setup-Hold Time Illustrations

Hold-1 case

Clock $t=0$ Data T_{Hold-1} Time

Clk-Q Delay T_{Clk-Q} T_{Rise-1} Time

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Other Latches/Registers: C²MOS

Master Stage Slave Stage

*Usually includes feedback to staticize

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C²MOS and Clock Overlap

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Other Latches/Registers: Pulse-Triggered Latches

Master-Slave Latches

Pulse-Triggered Latch

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Other Latches/Registers: TSPC

Positive latch
(transparent when CLK= 1)

Negative latch
(transparent when CLK= 0)

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Why not route the pulse?

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TSPC Operation

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Next Lecture

- Timing

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