# EE141-Fall 2012 Digital Integrated Circuits

Lecture 25
Clock Distribution



## Announcements

- Homework #8 due tomorrow
- Project phase 3 schedule
  - Now: poster Nov. 28th, report Dec. 3rd
  - Proposal: poster Dec. 3rd, report Dec. 7th
- Lectures next week:
  - Tues. lecture will be "taped ahead"
  - Thurs. lecture will be held "live" on Tues. Dec. 4th
  - HKN surveys will likely be held on the 4th as well



## Class Material

- Last lecture
  - Timing
- Today's lecture
  - Clock Distribution
- Reading
  - Chapter 10



# Clock Distribution



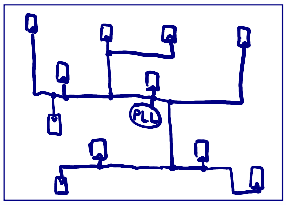
## Clock Distribution

- Single clock generally used to synchronize all logic on the same chip
  - Need to distribute clock over the entire die
  - While maintaining low skew/jitter
  - (And without burning too much power)

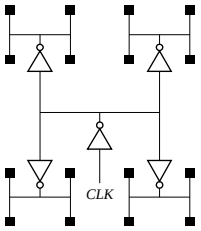


## Clock Distribution

- What's wrong with just routing wires to every point that needs a clock?



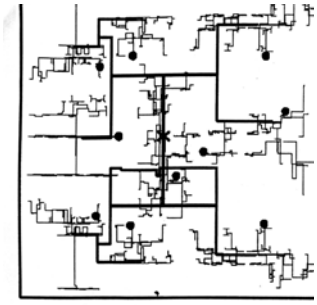
## H-Tree




Equal wire length/number of buffers to get to every location



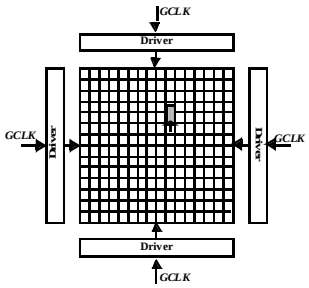
## More realistic H-tree



*[Restle98]*



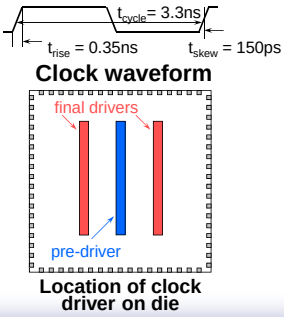
## Clock Grid




- *No RC matching*
- *But huge power*

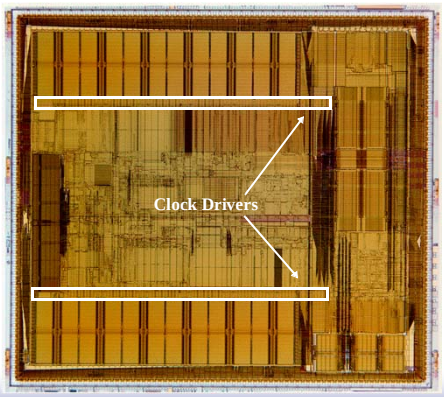


## Example: DEC Alpha 21164 (1995)



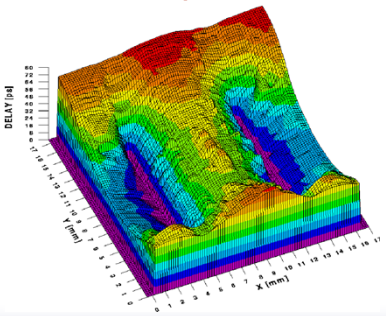

- 2 phase single wire clock, distributed globally
- 2 distributed driver channels
  - Reduced RC delay/skew
  - Improved thermal distribution
  - 3.75nF clock load, 20W power
  - 58 cm final driver width
- Local inverters for latching
- Conditional clocks in caches to reduce power
- More complex race checking
- Device variation



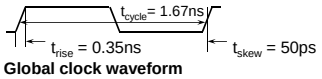




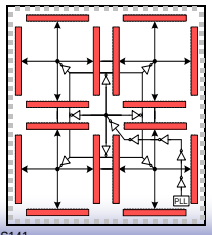

## Clock Skew in Alpha Processor



## EV6 (Alpha 21264) Clocking
## 600 MHz – 0.35 micron CMOS



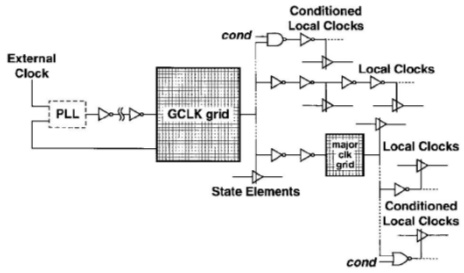

**Global clock waveform**




- 2 Phase, with multiple conditional buffered clocks
  - 2.8 nF clock load
  - 40 cm final driver width
- Local clocks can be gated "off" to save power
- Reduced load/skew
- Reduced thermal issues
- Multiple clocks complicate race checking

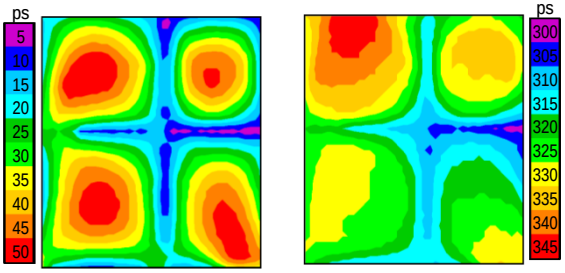


## 21264 Clocking






## EV6 Clock Results



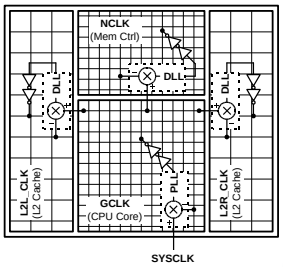

**GCLK Skew**
**(at Vdd/2 Crossings)**

**GCLK Rise Times**
**(20% to 80% Extrapolated to 0% to 100%)**



## EV7 Clock Hierarchy (2002)

***Active Skew Management and Multiple Clock Domains***



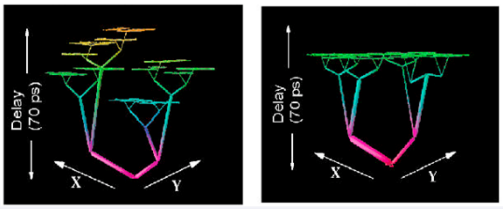

- **+ widely dispersed drivers**
- **+ DLLs compensate static and low-frequency variation**
- **+ divides design and verification effort**
- **- DLL design and verification is added work**
- **+ tailored clocks**



## Clock Animations

- By Phillip Restle (IBM)

http://www.research.ibm.com/people/r/restle/Animations/DAC01top.html






## Next Lecture

- Power distribution, I/O