EE141-Fall 2010 Digital Integrated Circuits

Lecture 26
I/O Issues
Power Distribution

Announcements

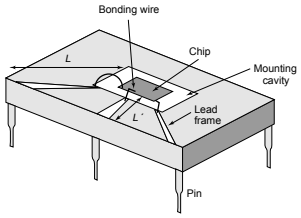
- Project phase 3
  - Poster session Mon. Dec. 3rd at 3:30pm
  - Final report: Fri. Dec. 7th 5:00pm
- Optional HW#9 posted
- HKN surveys in make-up lecture next Tues.
  - Please attend if you can

Class Material

- Last lecture
  - Clock distribution
- Today's lecture
  - I/O Design
  - Power Distribution

I/O Design

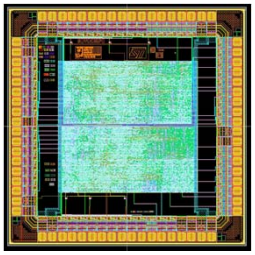
Chip Packaging



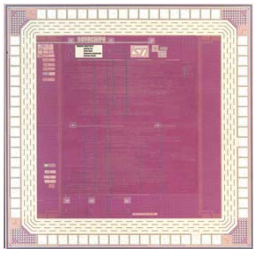
- Bond wires (~25μm) are used to connect the package to the chip
- Pads are arranged in a frame around the chip
- Pads are relatively large (~100μm in 0.25μm technology), with large pitch (100μm)
- Many chips are 'pad limited'

Pad Frame

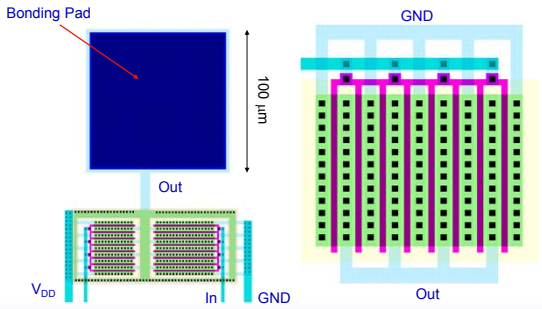
Layout



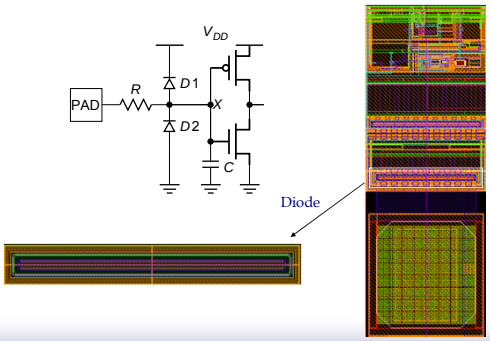
Die Photo



Bonding Pad Design

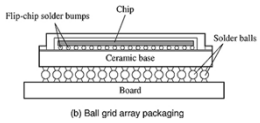


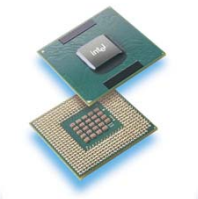
Pads + ESD Protection



Chip Packaging

- An alternative is 'flip-chip':
  - Pads are distributed around the chip
  - The solder balls are placed on pads
  - The chip is 'flipped' onto the package
  - Pads still large
    - But can have many more of them





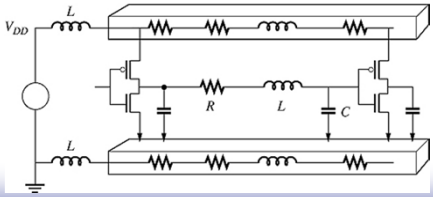
Power Distribution

ESD Protection

- When a chip is connected to a board, there is unknown (potentially large) static voltage difference
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.

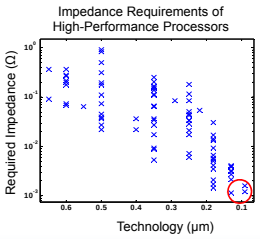
Power Supply Impedance

- No voltage source is ideal - ||Z|| > 0
- Two principal elements increase Z:
  - Resistance of supply lines (IR drop)
  - Inductance of supply lines (L·di/dt drop)



Scaling and Supply Impedance

- Typical target for supply impedance is to get 5-10% variation of nominal supply (e.g., 100mV for 1V supply)

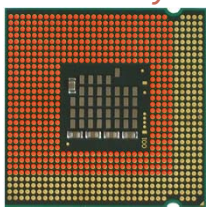


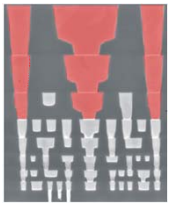
- In traditional scaling V_{dd} drops while power stays constant
- This forced drastic drop in supply impedance
  - V_{dd} ↓, I_{dd} ↑ → $|Z_{required}|$ ↓↓
- Today's chips:
  - $|Z_{required}| \approx 1\ m\Omega$!

IR Drop Example

- Intel Pentium 4: ~103W at ~1.275V
  - I_{dd} = 81Amps
- For 10% IR drop, total distribution resistance must be less than 1.6mΩ
- On-chip wire R ≈ 20mΩ/sq. (thick metal)
  - Can't meet R requirement even with multiple, complete layers dedicated to power
  - Main motivation for flip-chip packaging

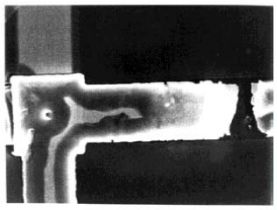
Power Delivery





- Achieving such low impedance requires a lot of resources:
  - ~70% of package pins just for power
  - Top 2-3 (thick) metal layers

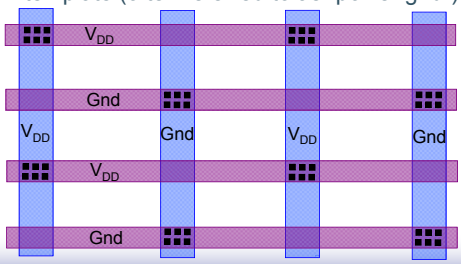
Not Just Impedance - Electromigration



- On-chip wires: current limited to ~1mA/μm for 5-7 year lifetime

On-Chip Power Distribution

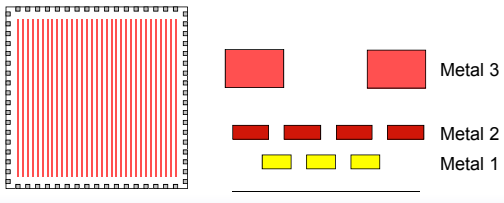
- Power network usually follows pre-defined template (often referred to as "power grid")



3 Metal Layer Approach (EV4)

3rd "coarse and thick" metal layer added to the technology for EV4 design

Power supplied from two sides of the die via 3rd metal layer
2nd metal layer used to form power grid
90% of 3rd metal layer used for power/clock routing

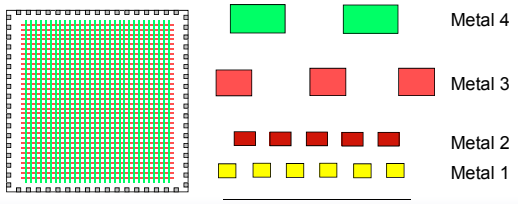


Courtesy Compaq

4 Metal Layers Approach (EV5)

4th "coarse and thick" metal layer added to the technology for EV5 design

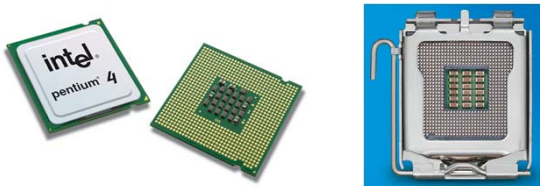
Power supplied from four sides of the die
Grid strapping done all in coarse metal
90% of 3rd and 4th metals used for power/clock routing



Courtesy Compaq

Decoupling Capacitors

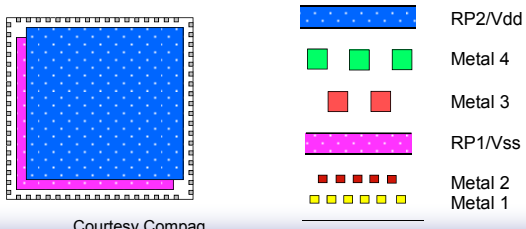
- Under the die



6 Metal Layer Approach – EV6

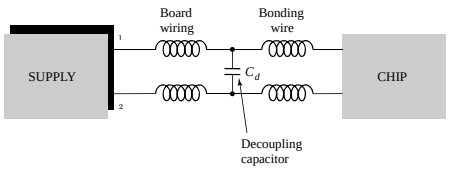
2 reference plane metal layers added to the technology for EV6 design

Solid planes dedicated to Vdd/Vss
Lowers on-chip inductance



Courtesy Compaq

Decoupling Capacitors



Decoupling capacitors are added:

- On the board (right under the supply pins)
- On the chip (under the supply straps, near large buffers)