



## *EE141-Fall 2012 Digital Integrated Circuits*

Lecture 27  
Flash and DRAM

## *Announcements*


- Project phase 3 final report due Friday
  - Send posters and reports to mailing list
  
- Final exam
  - Wed. Dec. 12<sup>th</sup>, 8-11am, Room TBA (see piazza)
  - Review session: Tues. Dec. 11<sup>th</sup> (stay tuned)
  
- HKN surveys end of class today

## *Announcements*

- GSI final review on Friday, Monday
  
- Look out for office hours announcements on the web

## *Class Material*

- Last lecture
  - I/O, power distribution
- Today's lecture
  - Flash memory
  - DRAM



## ROM and Flash

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## Read-Only Memory Cells

**1**

**Diode ROM**

**1**

**MOS ROM 1**

**1**

**MOS ROM 2**

**0**

**Diode ROM**

**0**

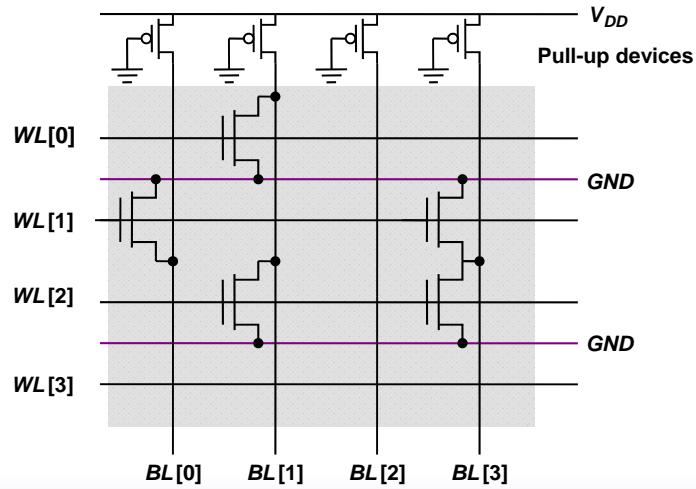
**MOS ROM 1**

**0**

**MOS ROM 2**

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## MOS NOR ROM

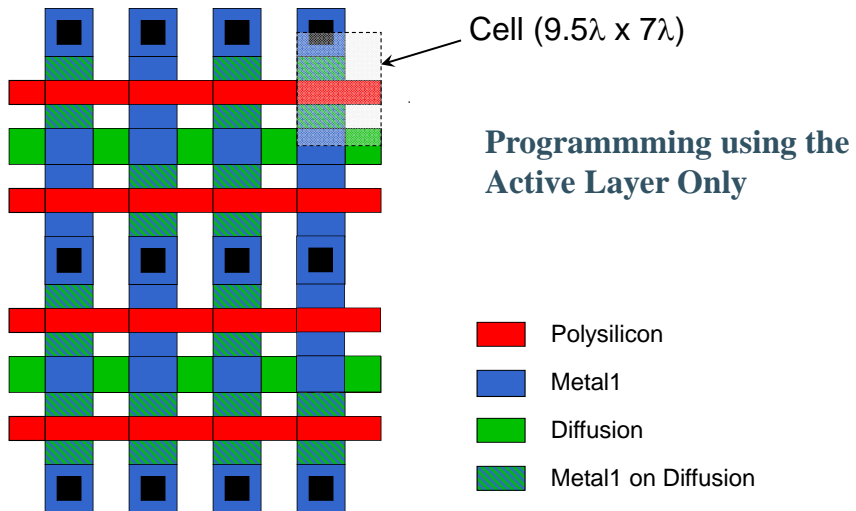


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## MOS NOR ROM Layout

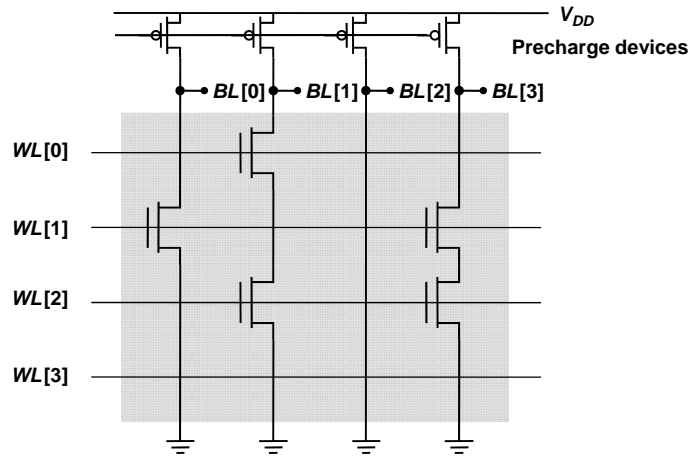


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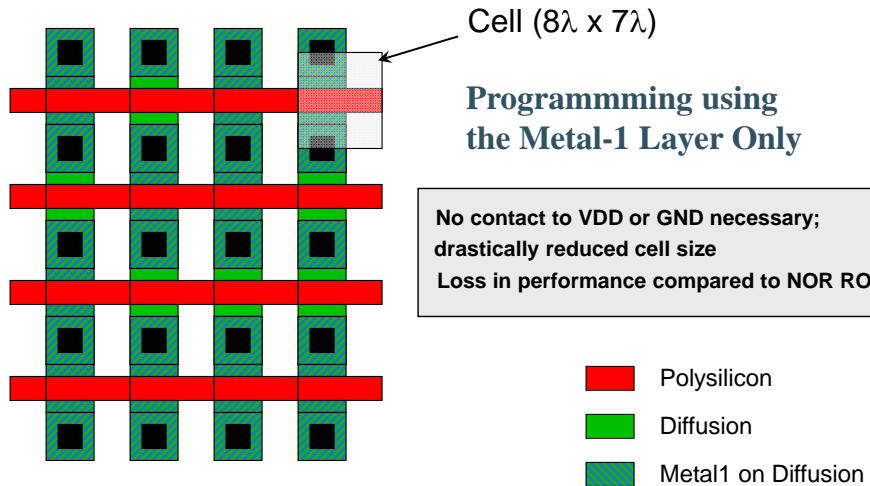
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## MOS NAND ROM

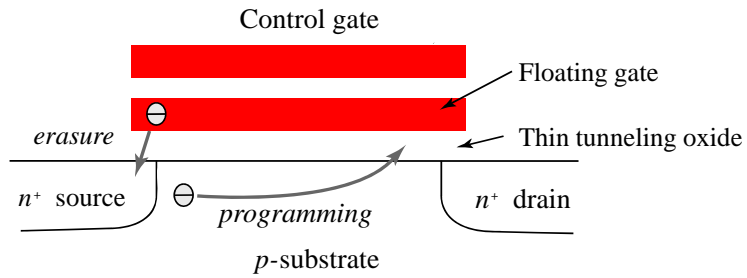


All word lines high by default with exception of selected row

## MOS NAND ROM Layout

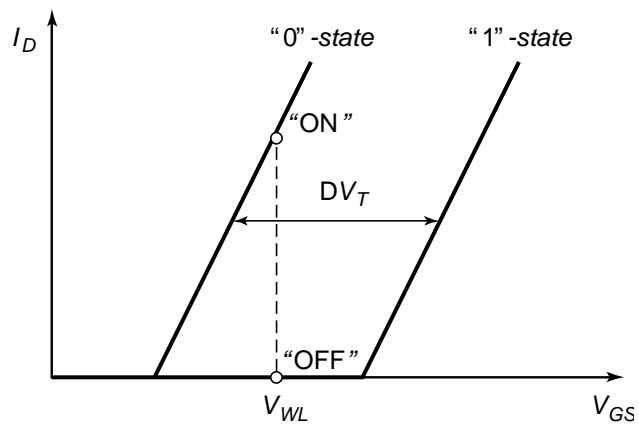


## Floating Gate Transistor

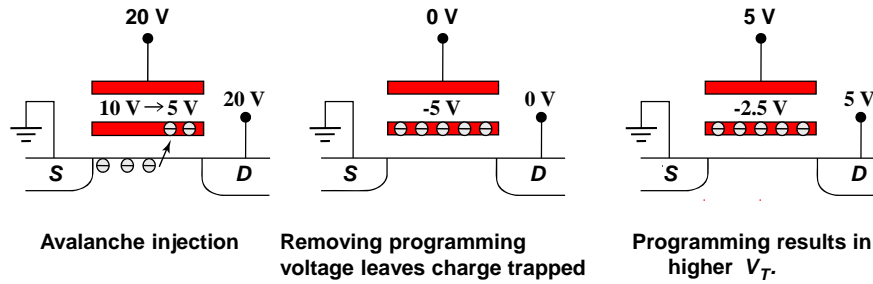


Many other options ...

## Programmable-Threshold

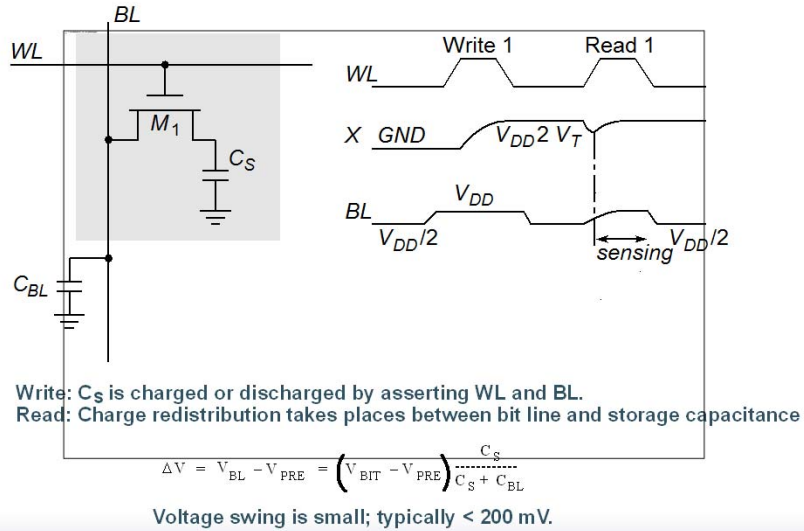


## *Floating-Gate Transistor Programming*



*DRAM*

## 1-Transistor DRAM Cell



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## DRAM Cell Observations

- 1T DRAM requires a sense amplifier
- Read-out of the 1T DRAM cell is destructive
  - Need refresh
- Lose a  $V_{TH}$  when writing a "1" into a DRAM cell
  - Bootstrap the word lines to a higher value than  $V_{DD}$

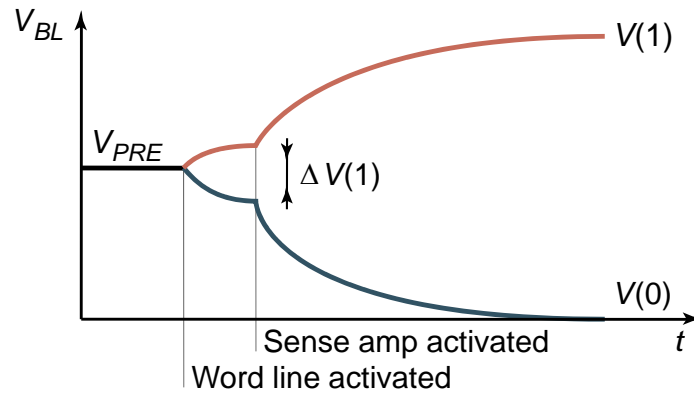
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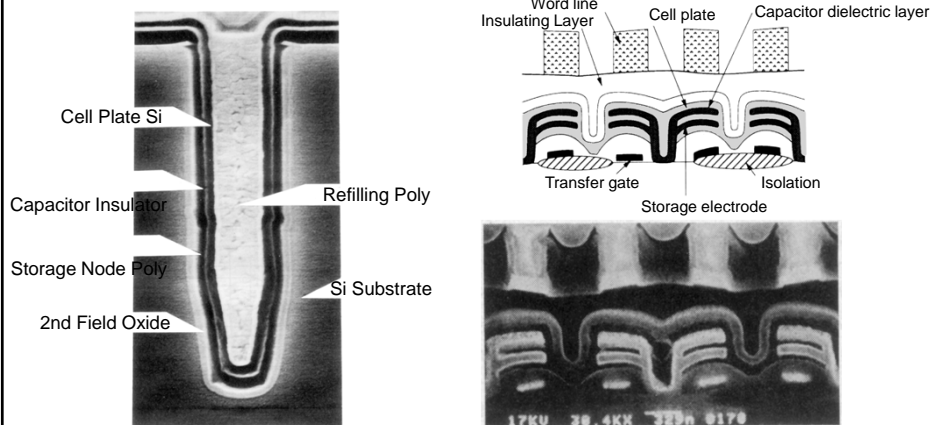
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## Sense Amp Operation



## Modern 1T1R DRAM Cells



Trench Cell

Stacked-capacitor Cell

*THE END*

□ This is just the beginning...