Lecture 27
Flash and DRAM

Announcements

- Project phase 3 final report due Friday
  - Send posters and reports to mailing list

- Final exam
  - Wed. Dec. 12th, 8-11am, Room TBA (see piazza)
  - Review session: Tues. Dec. 11th (stay tuned)

- HKN surveys end of class today
Announcements

- GSI final review on Friday, Monday
- Look out for office hours announcements on the web

Class Material

- Last lecture
  - I/O, power distribution
- Today’s lecture
  - Flash memory
  - DRAM
ROM and Flash

Read-Only Memory Cells

- Diode ROM
- MOS ROM 1
- MOS ROM 2
MOS NOR ROM

Pull-up devices


GND

V_{DD}

MOS NOR ROM Layout

Cell (9.5\lambda \times 7\lambda)

Programming using the Active Layer Only

Polysilicon
Metal1
Diffusion
Metal1 on Diffusion
**MOS NAND ROM**

All word lines high by default with exception of selected row

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**MOS NAND ROM Layout**

Cell (8λ x 7λ)

Programming using the Metal-1 Layer Only

No contact to VDD or GND necessary; drastically reduced cell size
Loss in performance compared to NOR ROM

- Polysilicon
- Diffusion
- Metal1 on Diffusion
**Floating Gate Transistor**

- Control gate
- Floating gate
- Thin tunneling oxide
- erasure
- programming
- $p$-substrate
- $n^+$ source
- $n^+$ drain

Many other options ...

**Programmable-Threshold**

- $I_D$ vs $V_{GS}$
- "0"-state
- "1"-state
- $V_{WL}$
- "ON"
- "OFF"
- $D_{VT}$
Floating-Gate Transistor Programming

Avalanche injection
Removing programming voltage leaves charge trapped
Programming results in higher $V_T$.

DRAM
1-Transistor DRAM Cell

![Diagram of 1-Transistor DRAM Cell]

Write: $C_S$ is charged or discharged by asserting $WL$ and $BL$.
Read: Charge redistribution takes place between bit line and storage capacitance.

\[ \Delta V = V_{BL} - V_{PRE} = \left( V_{RTT} - V_{PRE} \right) \frac{C_S}{C_S + C_{BL}} \]

Voltage swing is small; typically < 200 mV.

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DRAM Cell Observations

- 1T DRAM requires a sense amplifier
- Read-out of the 1T DRAM cell is destructive
  - Need refresh
- Lose a $V_{TH}$ when writing a “1” into a DRAM cell
  - Bootstrap the word lines to a higher value than $V_{DD}$
Sense Amp Operation

\[ V(1) \]

\[ \Delta V(1) \]

Sense amp activated

Word line activated

Modern 1T DRAM Cells

Trench Cell

Stacked-capacitor Cell
THE END

- This is just the beginning…