



*EE141-Fall 2012
Digital Integrated
Circuits*

Lecture 27
Flash and DRAM

EECS141 Lecture #27 1

Class Material


- Last lecture
 - I/O, power distribution
- Today's lecture
 - Flash memory
 - DRAM

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Announcements

- Project phase 3 final report due Friday
 - Send posters and reports to mailing list
- Final exam
 - Wed. Dec. 12th, 8-11am, Room TBA (see piazza)
 - Review session: Tues. Dec. 11th (stay tuned)
- HKN surveys end of class today

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ROM and Flash

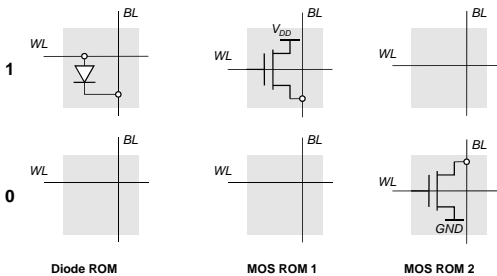
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Announcements

- GSI final review on Friday, Monday
- Look out for office hours announcements on the web

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Read-Only Memory Cells

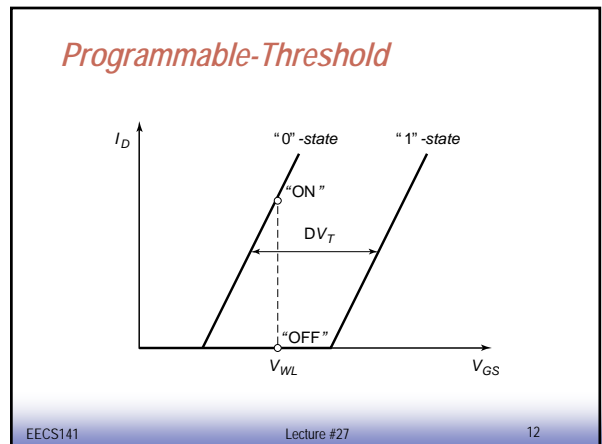
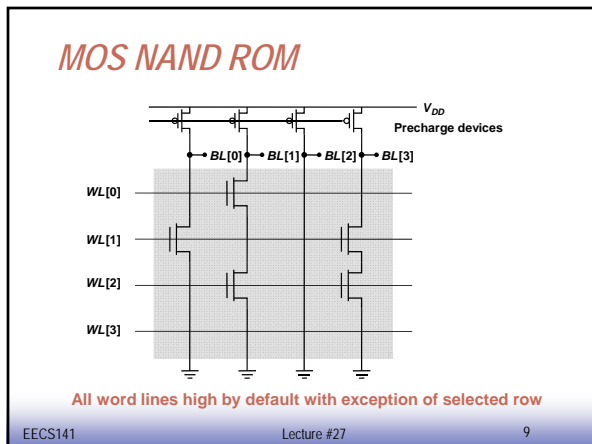
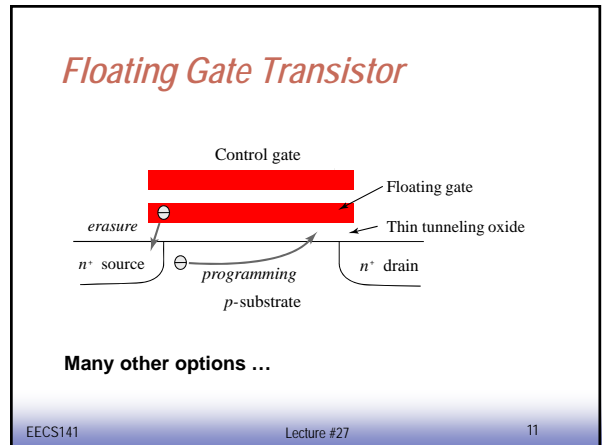
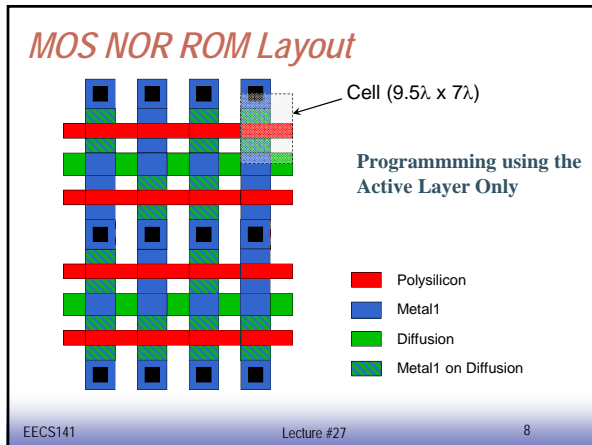
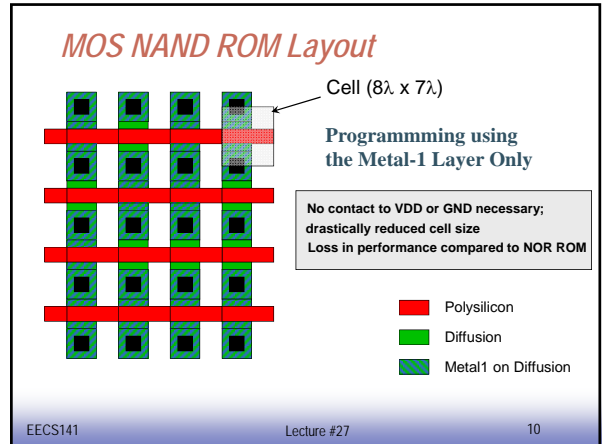
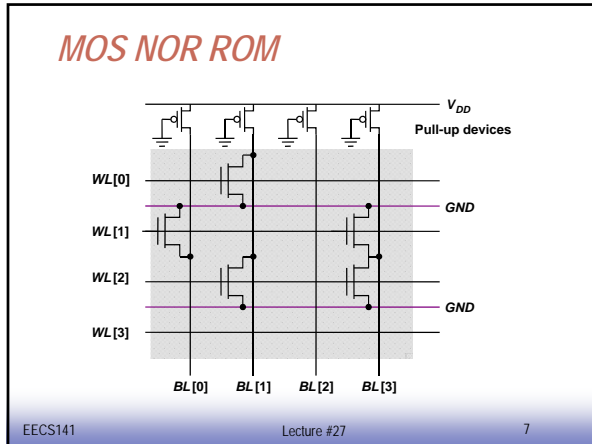


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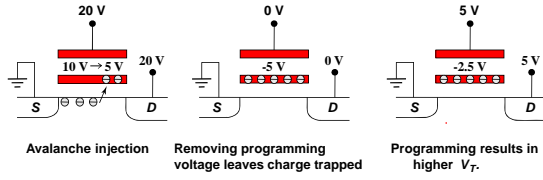
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Diode ROM MOS ROM 1 MOS ROM 2

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Floating-Gate Transistor Programming



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DRAM Cell Observations

- 1T DRAM requires a sense amplifier
- Read-out of the 1T DRAM cell is destructive
 - Need refresh
- Lose a V_{TH} when writing a "1" into a DRAM cell
 - Bootstrap the word lines to a higher value than V_{DD}

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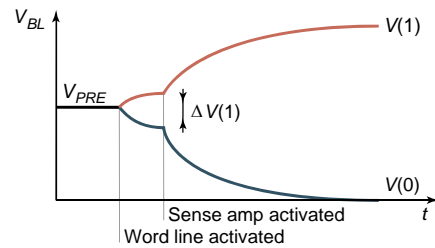
DRAM

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Sense Amp Operation

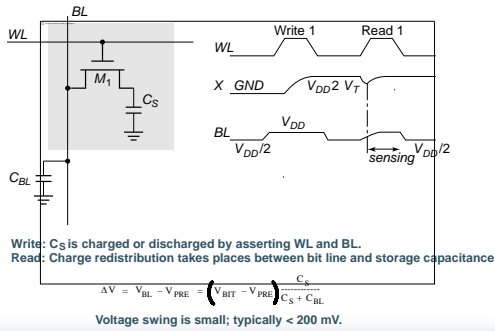


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1-Transistor DRAM Cell

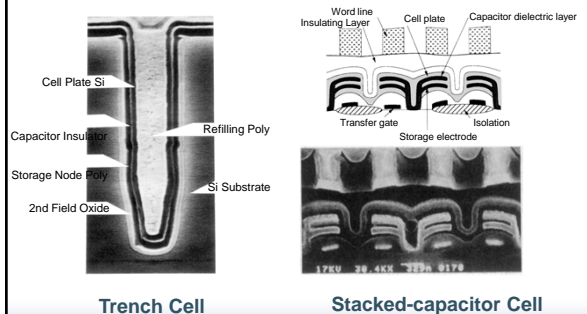


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Modern 1T DRAM Cells



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THE END

□ This is just the beginning...