Administrative Stuff

- Discussions start tomorrow (Fri.)
- Labs start next week
  - Everyone should have an EECS instructional account
- Homework #1 is due today
- Homework #2 due next Thursday
Class Material

- Last lecture
  - Basics of IC manufacturing, cost
- Today's lecture
  - Transistor as switches
  - Building an inverter
  - Design metrics

What is a Transistor?

An MOS Transistor

A Switch!

\[ |V_{GS}| \geq |V_T| \]

\[ V_{GS} \]

S D G

\[ R_{on} \]

S \hspace{1cm} D
Switch Model of MOS Transistor

\[ |V_{GS}| < |V_T| \] and \[ |V_{GS}| > |V_T| \]

NMOS and PMOS

NMOS Transistor: \[ V_{GS} > 0 \]  
PMOS Transistor: \[ V_{GS} < 0 \]
Building a CMOS inverter

Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Speed/Performance (delay, frequency)
  - Power
Reliability

- The real world is analog
  - All physical quantities you deal with as a circuit designer are actually continuous
- Thus, even a “digital” signal can be noisy:

Noise and Digital Systems

- Circuit needs to work despite “analog” noise
  - Digital gates can reject noise
  - This is actually how digital systems are defined
- Digital system is one where:
  - Discrete values mapped to analog levels and back
  - All the elements (gates) can reject noise
    - For “small” amounts of noise, output noise is less than input noise
  - Thus, for sufficiently “small” noise, the system acts as if it was noiseless
**Noise Rejection**

- To see if a gate rejects noise:
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0

- Ideal digital gate:
  - Noise needs to be larger than $V_{DD}/2$ to have any effect on gate output

\[
\text{Gain} = \begin{cases} 
0 & \text{if input is exactly 0 or 1} \\
\infty & \text{otherwise}
\end{cases}
\]

**More Realistic VTC**

- $V_{OH} = f(V_{OL})$
- $V_{OL} = f(V_{OH})$
- $V_{ML} = f(V_{ML})$

**Switching Threshold**

- Nominal Voltage Levels
**Voltage Mapping**

- "1": $V_{OH}$, $V_{IH}$, Undefined Region
- "0": $V_{IL}$, $V_{OL}$

Graph:
- Slope = -1

**Definition of Noise Margins**

Gate Output (Stage M) → Gate Input (Stage M+1)

- Noise margin high: $NM_H = V_{OH} - V_{IH}$
- Noise margin low: $NM_L = V_{IL} - V_{OL}$
**Digital Gate Noise Reduction: Regenerative Property**

A chain of inverters

![Simulated response graph](image)

**Regenerative Property (Another View)**

Regenerative

Non-Regenerative
Fan-in and Fan-out

There is a modified definition of fan-out for CMOS logic.

Key Reliability Properties

- Absolute noise margin values are not the only things that matter
  - e.g., floating (high impedance) nodes are more easily disturbed than low impedance nodes (in terms of voltage)
- Noise immunity (i.e., how well the gate suppresses noise sources) needs to be considered too

Summary of some key reliability metrics:
- Noise transfer functions & margin (ideal: gain = ∞, margin = \( V_{dd}/2 \))
- Output impedance (ideal: \( R_o = 0 \))
- Input impedance (ideal: \( R_i = ∞ \))
Example: An Old-time Inverter

\[ V_{OH} = 3.6\text{V} \]
\[ V_{OL} = 0.4\text{V} \]
\[ V_{IL} = 0.6\text{V} \]
\[ V_{IH} = 2.3\text{V} \]
\[ NM_H = V_{OH} - V_{IH} = 1.3\text{V} \]
\[ NM_L = V_{IL} - V_{OL} = 0.2\text{V} \]
Fanout of Four (FO4) Delay

- Want a way to characterize the delay of a circuit (roughly) independent of technology

- Most common metric:
  - Delay of an inverter driving four copies of itself ($t_{\text{FO4}}$)
A First-Order RC Network

$$v_{out}(t) = (1 - e^{-t/\tau}) \cdot V$$

$$t_p = \ln (2) \tau = 0.69 \cdot RC$$

Important model – matches delay of an inverter

Power Dissipation

Instantaneous power:
$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:
$$P_{peak} = V_{supply}i_{peak}$$

Average power:
$$P_{ave} = \frac{1}{T} \int_t^{t+T} p(t)dt = \frac{V_{supply}}{T} \int_t^{t+T} i_{supply}(t)dt$$
“Power-Delay” and Energy-Delay

- Want low power and low delay, so how about optimizing the product of the two?
  - So-called “Power-Delay Product”

- Power·Delay is by definition Energy
  - Optimizing this pushes you to go as slow as possible

- Alternative gate metric: Energy-Delay Product
  - EDP = (P_{av}·t_p)·t_p = E·t_p

Energy in CMOS

- The voltage on $C_L$ eventually settles to $V_{DD}$
- Thus, charge stored on the capacitor is $C_LV_{DD}$
  - This charge has to flow out of the power supply
- So, energy is just $Q · V_{DD} = (C_LV_{DD}) · V_{DD}$
Energy (the harder way)

\[ E_{0 \rightarrow 1} = \int_{0}^{T} P_{DD}(t) \, dt = V_{DD} \int_{0}^{T} i_{DD}(t) \, dt = V_{DD} \int_{0}^{V_{DD}} C_L \, dV_{out} = C_L V_{DD}^2 \]

\[ E_C = \int_{0}^{T} P_C(t) \, dt = \int_{0}^{T} V_{out} i_L(t) \, dt = \int_{0}^{V_{DD}} C_L V_{out} \, dV_{out} = \frac{1}{2} C_L V_{DD}^2 \]

Energy Thought Experiment (1)

- Why doesn’t R matter?
Energy Thought Experiment (2)

- Where did the energy go?

![Energy Diagram]

\[ E_{\text{vin}} = C_L V_{\text{in}}^2 \]
\[ E_{\text{CL}} = \frac{1}{2} C_L V_{\text{in}}^2 \]

Summary

- Understanding the design metrics that govern digital design is crucial
  - Cost
  - Robustness
  - Performance/speed
  - Power and energy dissipation
Next Lecture

- Detailed CMOS switch model
- Building gates with switches
- Design rules