EE141-Fall 2012 Digital Integrated Circuits

Lecture 3
Switches, Inverters, and Design Metrics

Administrative Stuff

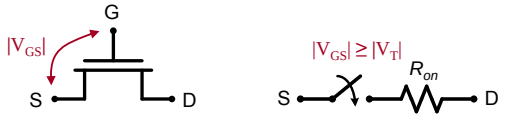
- Discussions start tomorrow (Fri.)
- Labs start next week
  - Everyone should have an EECS instructional account
- Homework #1 is due today
- Homework #2 due next Thursday

Class Material

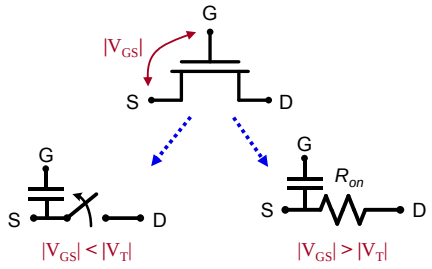
- Last lecture
  - Basics of IC manufacturing, cost
- Today's lecture
  - Transistor as switches
  - Building an inverter
  - Design metrics

What is a Transistor?

An MOS Transistor ⟷ A Switch!

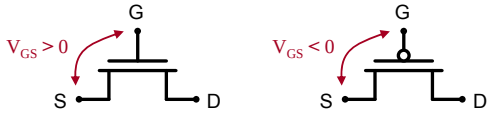


Switch Model of MOS Transistor



NMOS and PMOS

NMOS Transistor PMOS Transistor



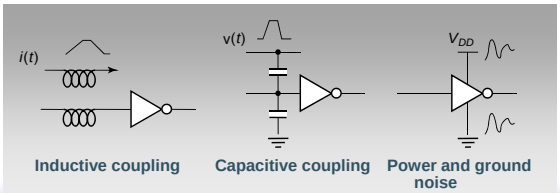
Building a CMOS inverter

Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Speed/Performance (delay, frequency)
  - Power

Reliability

- The real world is analog
  - All physical quantities you deal with as a circuit designer are actually continuous
- Thus, even a "digital" signal can be noisy:

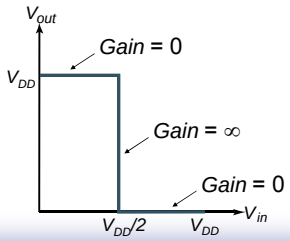


Noise and Digital Systems

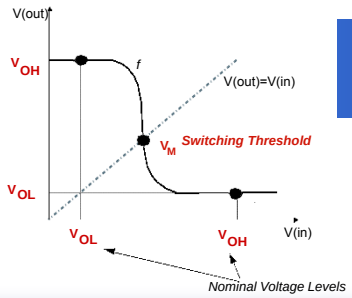
- Circuit needs to works despite "analog" noise
  - Digital gates can reject noise
  - This is actually how digital systems are defined
- Digital system is one where:
  - Discrete values mapped to analog levels and back
  - All the elements (gates) can reject noise
    - For "small" amounts of noise, output noise is less than input noise
  - Thus, for sufficiently "small" noise, the system acts as if it was noiseless

Noise Rejection

- To see if a gate rejects noise
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0
- Ideal digital gate:
  - Noise needs to be larger than $V_{DD}/2$ to have any effect on gate output

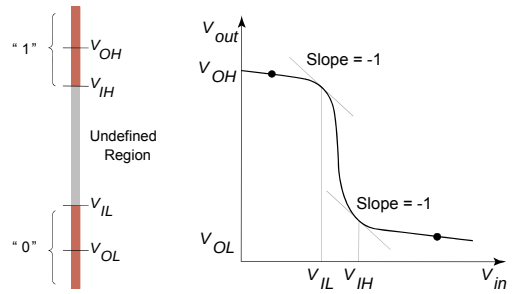


More Realistic VTC

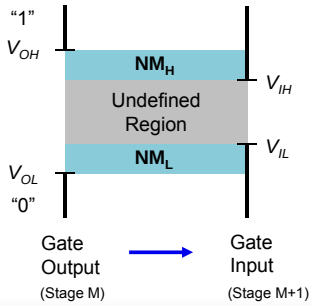


VOH = *f*(VOL)
VOL = *f*(VOH)
VM = *f*(VM)

Voltage Mapping



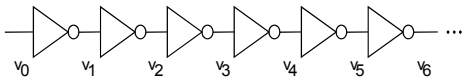
Definition of Noise Margins



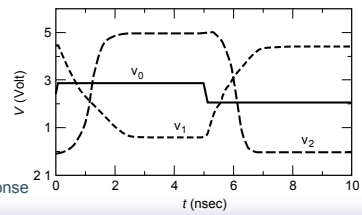
Noise margin high:
$NM_H = V_{OH} - V_{IH}$

Noise margin low:
$NM_L = V_{IL} - V_{OL}$

Digital Gate Noise Reduction: Regenerative Property

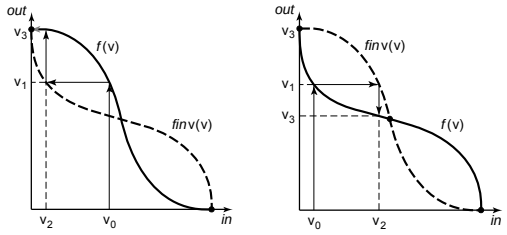


A chain of inverters

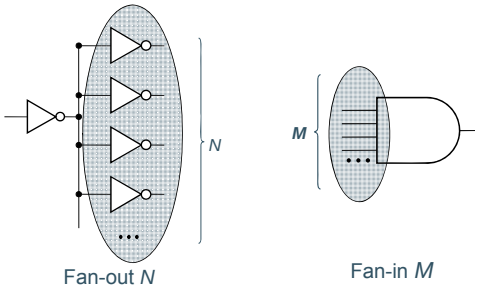


Simulated response

Regenerative Property (Another View)



Fan-in and Fan-out

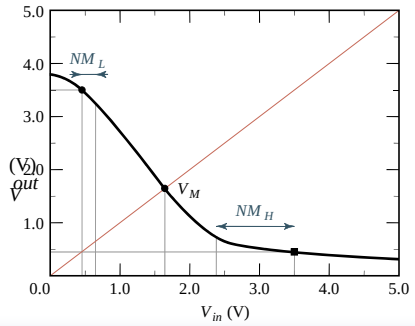


There is a modified definition of fan-out for CMOS logic

Key Reliability Properties

- Absolute noise margin values are not the only things that matter
  - e.g., floating (high impedance) nodes are more easily disturbed than low impedance nodes (in terms of voltage)
- Noise immunity (i.e., how well the gate suppresses noise sources) needs to be considered too
- Summary of some key reliability metrics:
  - Noise transfer functions & margin (ideal: gain = ∞, margin = $V_{dd}/2$)
  - Output impedance (ideal: $R_o = 0$)
  - Input impedance (ideal: $R_i = \infty$)

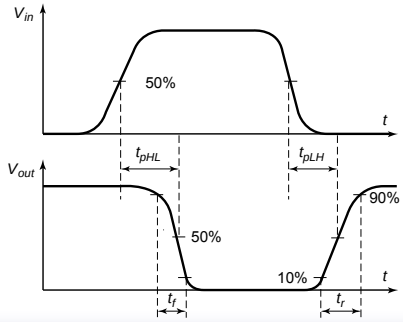
Example: An Old-time Inverter



Example: An Old-time Inverter

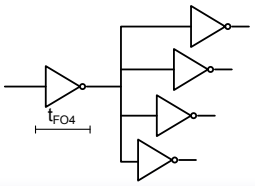
- V_{OH} = 3.6V
- V_{OL} = 0.4V
- V_{IL} = 0.6V
- V_{IH} = 2.3V
- $NM_H = V_{OH} - V_{IH}$ = 1.3V
- $NM_L = V_{IL} - V_{OL}$ = 0.2V

Performance: Delay Definitions

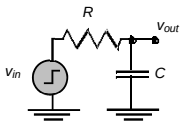


Fanout of Four (FO4) Delay

- Want a way to characterize the delay of a circuit (roughly) independent of technology
- Most common metric:
  - Delay of an inverter driving four copies of itself (t_{FO4})



A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau})\ V$$

$$t_p = \ln(2)\ \tau = 0.69\ RC$$

Important model – matches delay of an inverter

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

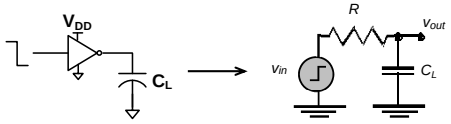
Average power:

$$P_{ave} = \frac{1}{T}\int_t^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_t^{t+T} i_{supply}(t)dt$$

"Power-Delay" and Energy-Delay

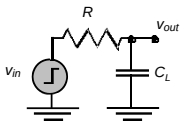
- Want low power and low delay, so how about optimizing the product of the two?
  - So-called "Power-Delay Product"
- Power·Delay is by definition Energy
  - Optimizing this pushes you to go as slow as possible
- Alternative gate metric: Energy-Delay Product
  - EDP = $(P_{av} \cdot t_p) \cdot t_p = E \cdot t_p$

Energy in CMOS



- The voltage on C_L eventually settles to V_{DD}
- Thus, charge stored on the capacitor is $C_L V_{DD}$
  - This charge has to flow out of the power supply
- So, energy is just $Q \cdot V_{DD} = (C_L V_{DD}) \cdot V_{DD}$

Energy (the harder way)



$$E_{0\to 1} = \int_0^T P_{DD}(t)dt = V_{DD}\int_0^T i_{DD}(t)dt = V_{DD}\int_0^{V_{DD}} C_L dv_{out} = C_L V_{DD}^2$$

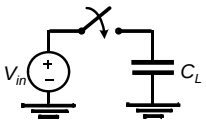
$$E_C = \int_0^T P_C(t)dt = \int_0^T v_{out} i_L(t)dt = \int_0^{V_{DD}} C_L v_{out} dv_{out} = \frac{1}{2} C_L V_{DD}^2$$

Energy Thought Experiment (1)

- Why doesn't R matter?

Energy Thought Experiment (2)

- Where did the energy go?



$E_{Vin} = C_L V_{in}^2$

$E_{CL} = (1/2) C_L V_{in}^2$

Summary

- Understanding the design metrics that govern digital design is crucial
  - Cost
  - Robustness
  - Performance/speed
  - Power and energy dissipation

Next Lecture

- Detailed CMOS switch model
- Building gates with switches
- Design rules