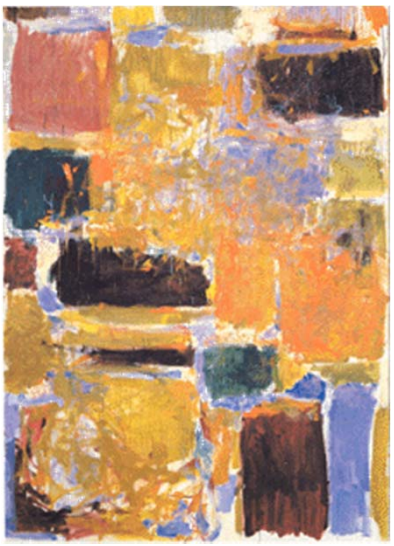


# EE141-Fall 2012 Digital Integrated Circuits

Lecture 4
CMOS Switches and Gates
Design Rules



## Administrative Stuff

- Labs start this week
  - Software lab #2 starts today
  - Lab reports due the following week in lab
- Homework #2 due this Thurs.
  - Homework #3 out this Thurs.

## Review: Delay

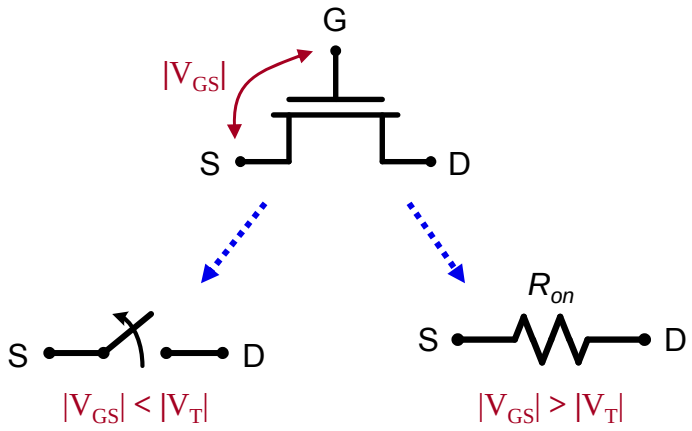
- Is it possible for a gate to have negative delay?



## Class Material

- Last lecture
  - Transistor as a switch, inverter
  - Design metrics
- Today's lecture
  - Detailed switch model
  - CMOS gates (intro to Ch. 3, 6)
  - Design rules (Ch. 2.3)
- Reading (2.3, 3.3.1-3.3.2, 6.1-6.2.1)

## Switch Model of MOS Transistor



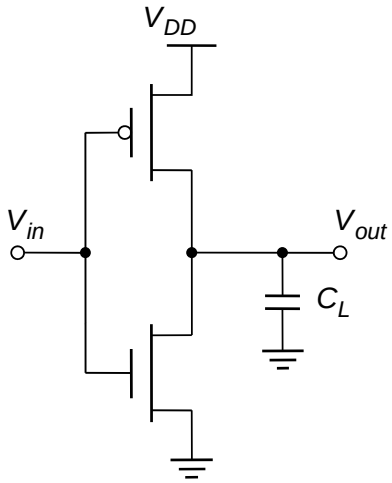


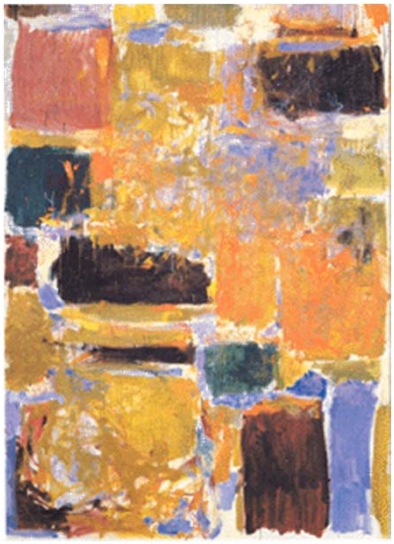

## MOS Switch Model (Capacitance)

## Switch Model (Width)



## CMOS Inverter Model

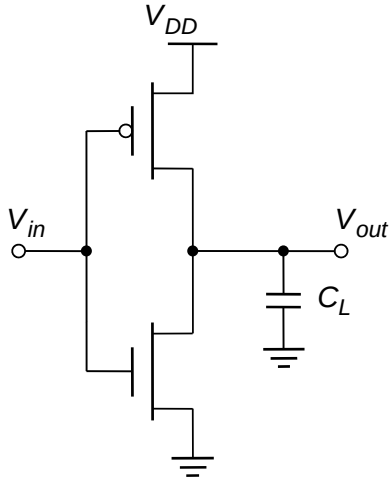




# CMOS Logic



# The CMOS Inverter: A First Glance



## Static CMOS Gates

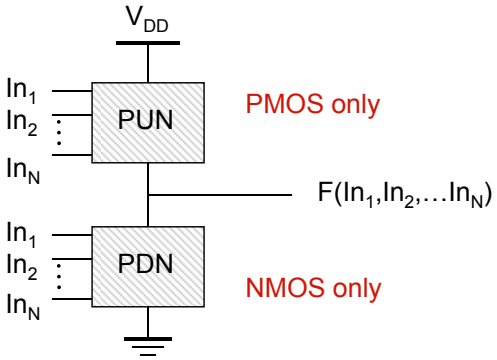
At every point in time (except during the switching transients) each gate output is connected to either $V_{DD}$ or $V_{SS}$ via a low resistive path.

The outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring, once again, the transient effects during switching periods).

(Will contrast this later to dynamic circuit style.)

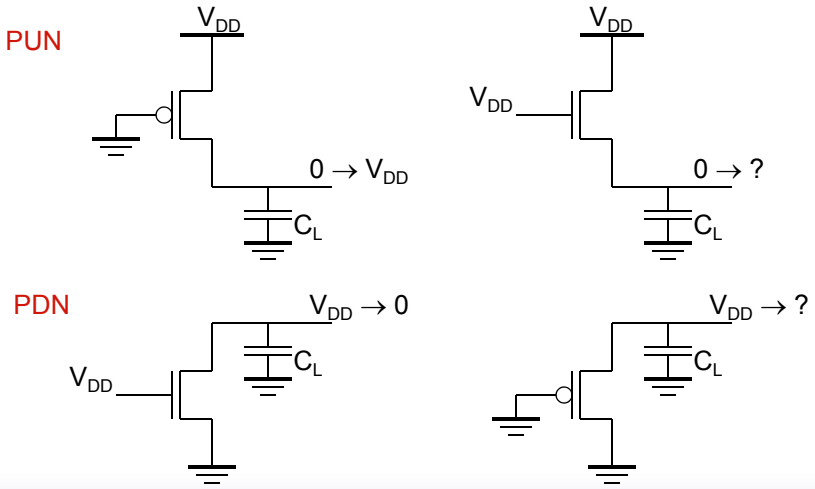


## Static Complementary CMOS




PUN and PDN are dual logic networks
PUN and PDN functions are complementary

## Threshold Drops

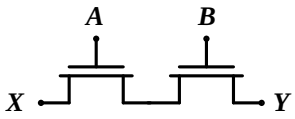





## NMOS Transistors in Series/Parallel Connection

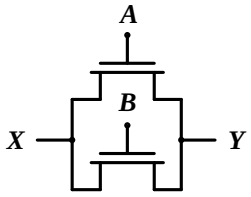
- Transistor ↔ switch controlled by its gate signal
  - NMOS switch on when switch control input is high

**AND**




***Y* = *X* if *A* AND *B***

**OR**



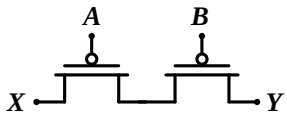

***Y* = *X* if *A* OR *B***

- NMOS transistors pass a “strong” 0 but a “weak” 1

## PMOS Transistors in Series/Parallel Connection

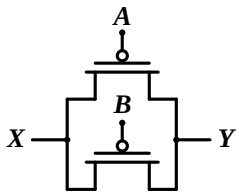
- PMOS switch on when switch control is low

**NOR**




$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$

**NAND**




$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

- PMOS transistors pass a "strong" 1 but a "weak" 0



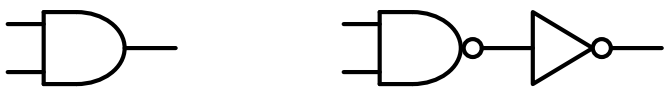
## Complementary CMOS Logic Style

- PUP is the **dual** to PDN
  (can be shown using DeMorgan's Theorems)

$$\overline{A + B} = \overline{A}\,\overline{B}$$

$$\overline{AB} = \overline{A} + \overline{B}$$

- Static CMOS gates are always inverting

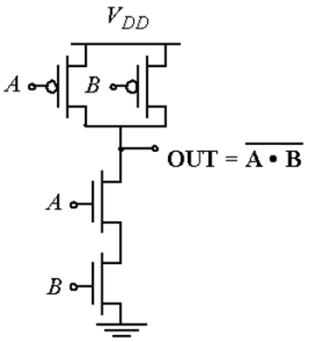


**AND = NAND + INV**

# Example Gate: NAND

| A | B | Out |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Truth Table of a 2 input NAND gate



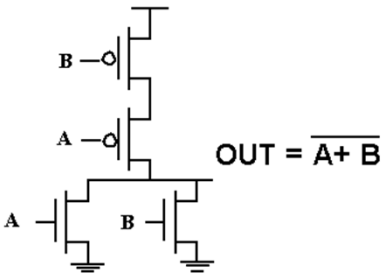

- PDN: G = AB $\Rightarrow$ Conduction to GND
- PUN: F = $\overline{A}$ + $\overline{B}$ = $\overline{AB}$ $\Rightarrow$ Conduction to $V_{DD}$
- $\overline{G(In_1,In_2,In_3,\ldots)} \equiv F(\overline{In_1},\overline{In_2},\overline{In_3},\ldots)$



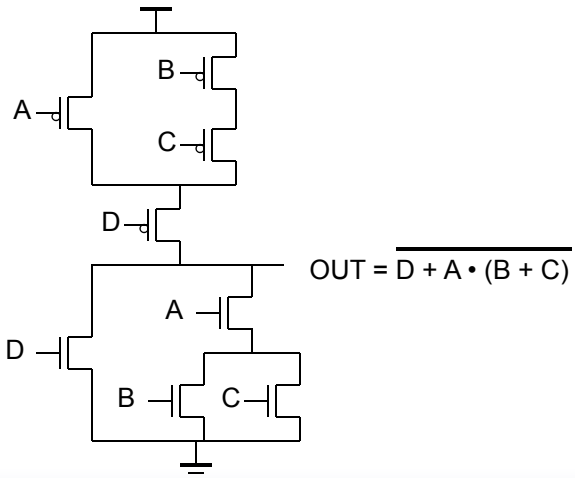
# Example Gate: NOR

| A | B | Out |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Truth Table of a 2 input NOR gate



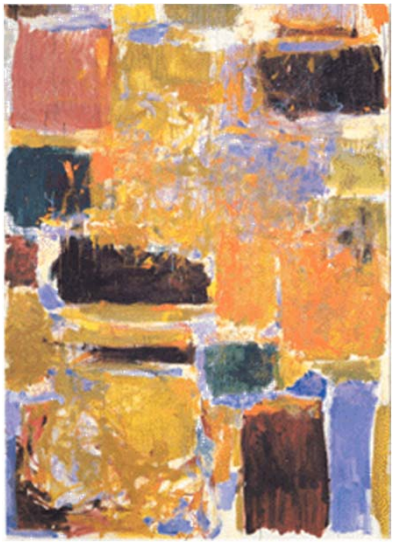
## Complex CMOS Gate






## CMOS Properties

- Full rail-to-rail swing
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation

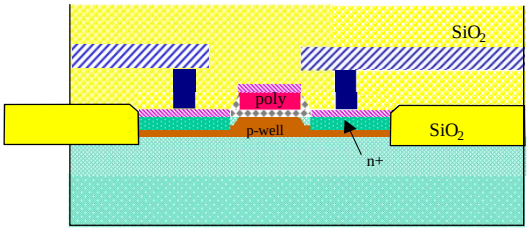


# Design Rules

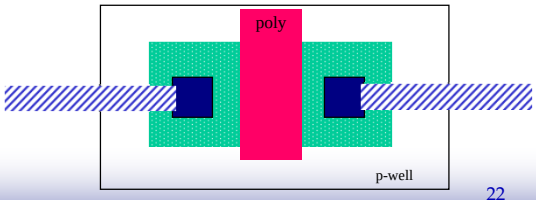


# Transistor Layout

Cross-Sectional View




Layout View

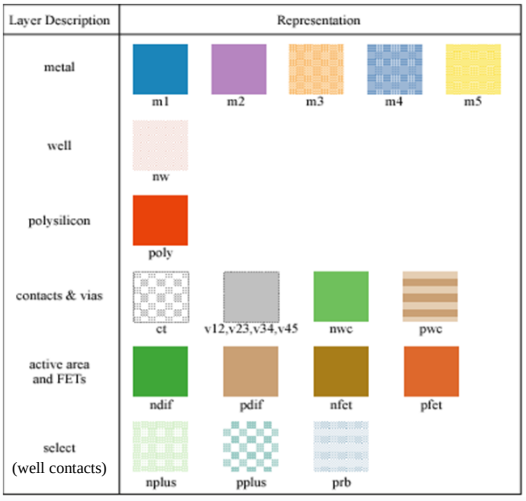


# CMOS Process Layers

| Layer | Color | Representation |
|---|---|---|
| Well (p,n) | Yellow | |
| Active Area (n+,p+) | Green | |
| Well contact (p+,n+) | Green | |
| Polysilicon | Red | |
| Metal1 | Blue | |
| Metal2 | Magenta | |
| Contact To Poly | Black | |
| Contact To Diffusion | Black | |
| Via | Black | |



# Layers in 0.25 μm CMOS process



## Design Rules

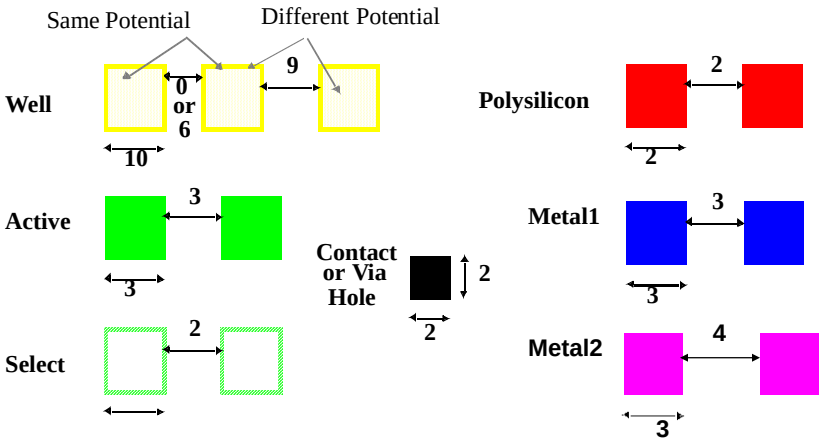
- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)



## Design Rules

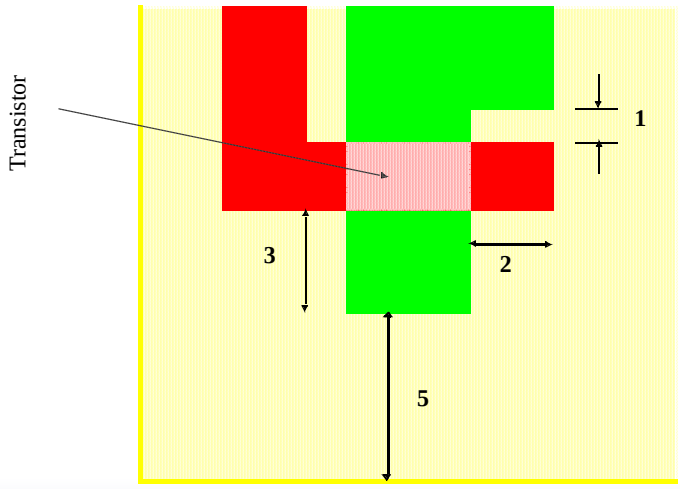
- Intra-layer
  - Widths, spacing, area
- Inter-layer
  - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

# Intra-Layer Design Rules

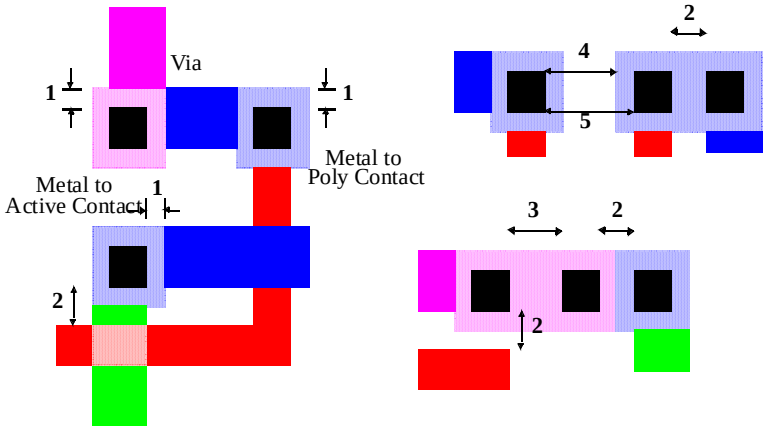





# Inter-Layer: Transistor Layout

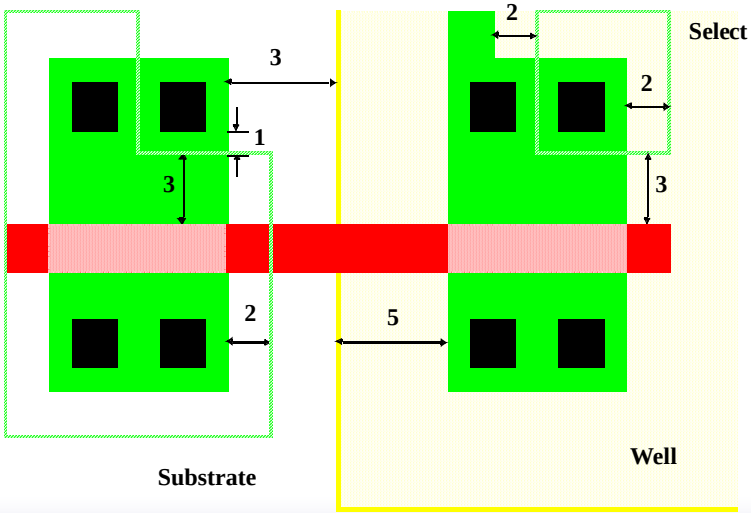


# Inter-Layer: Vias and Contacts

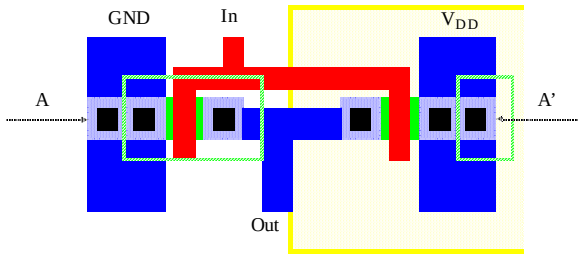




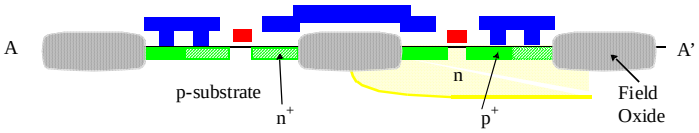

# Inter-Layer: Well and Substrate



# CMOS Inverter Layout




(a) Layout




(b) Cross-Section along A-A'



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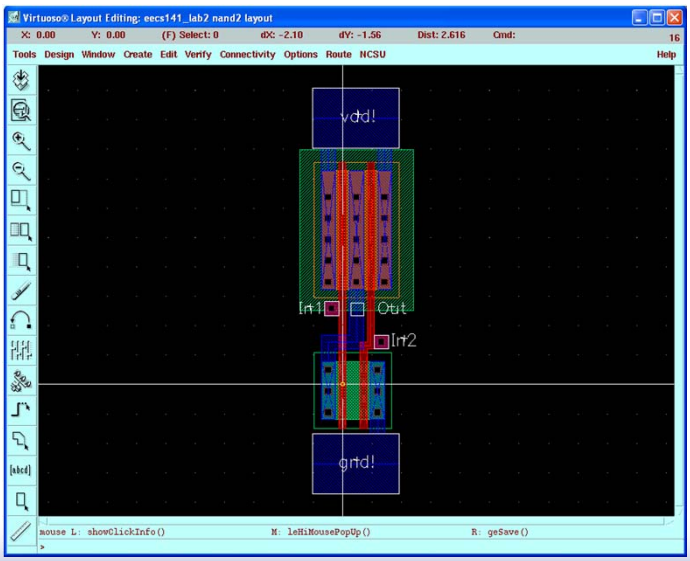
# Layout Editor



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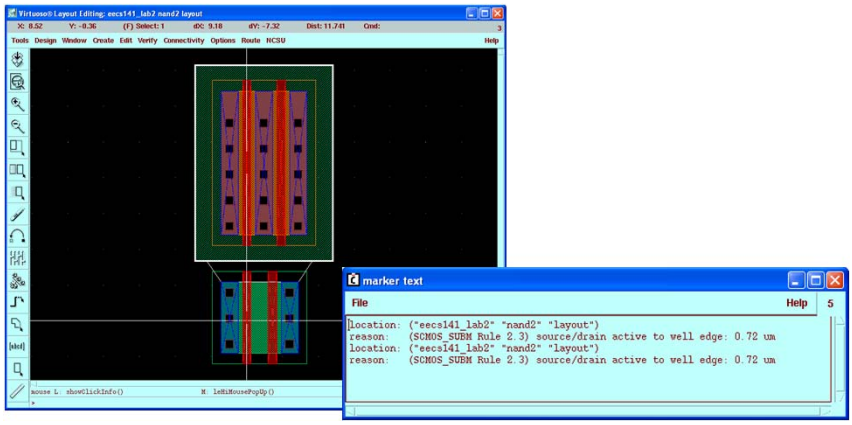
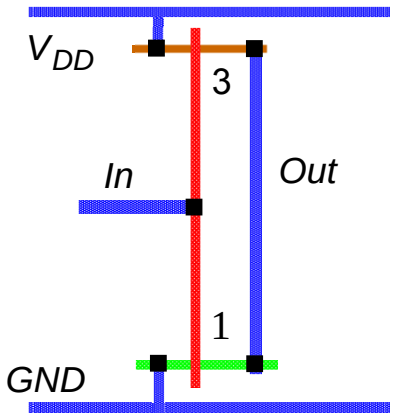
## Design Rule Checker






## Layout vs. Schematic (LVS)

# Stick Diagram

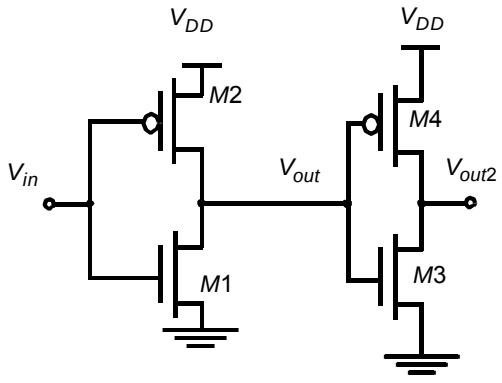



- Dimensionless layout entities
- Only topology is important

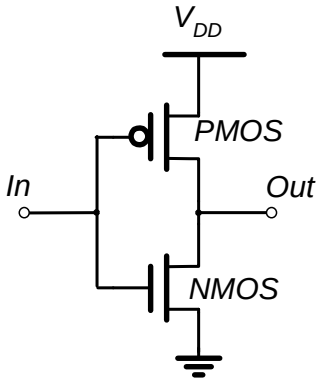
**Stick diagram of inverter**

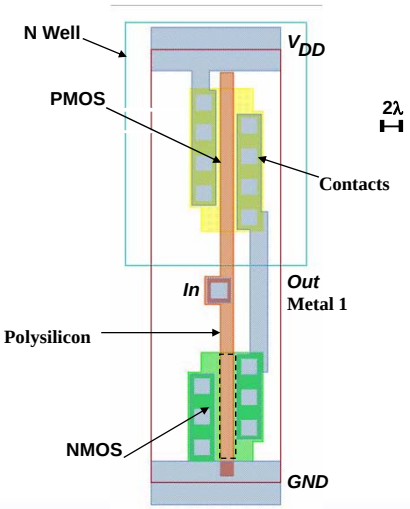


# Circuit Under Design



# CMOS Inverter



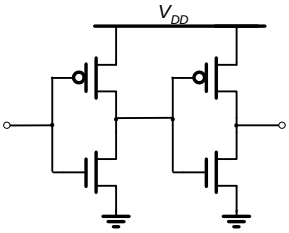



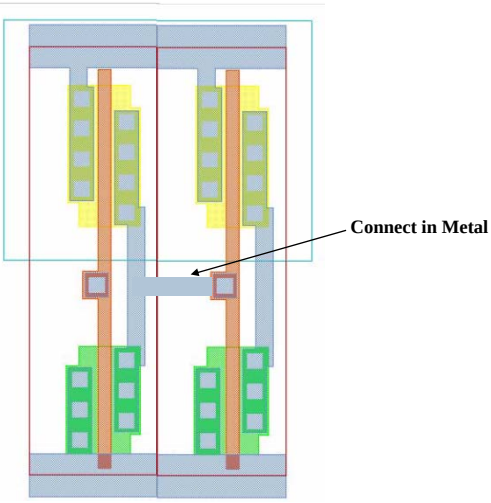



# Two Inverters

Share power and ground

Abut cells



## *Next Lecture*

- Overview of semiconductor memory