



EE141-Fall 2012 Digital Integrated Circuits

Lecture 4
CMOS Switches and Gates
Design Rules

Administrative Stuff

- Labs start this week
 - Software lab #2 starts today
 - Lab reports due the following week in lab

- Homework #2 due this Thurs.
 - Homework #3 out this Thurs.

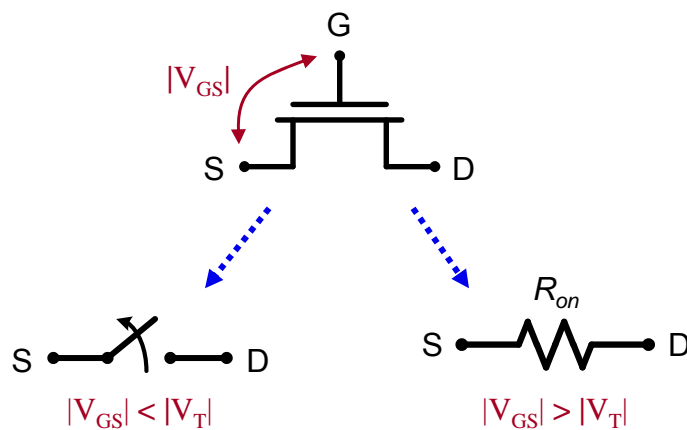
Review: Delay

- Is it possible for a gate to have negative delay?

Class Material

- Last lecture
 - Transistor as a switch, inverter
 - Design metrics
- Today's lecture
 - Detailed switch model
 - CMOS gates (intro to Ch. 3, 6)
 - Design rules (Ch. 2.3)
- Reading (2.3, 3.3.1-3.3.2, 6.1-6.2.1)

Switch Model of MOS Transistor



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MOS Switch Model (Capacitance)

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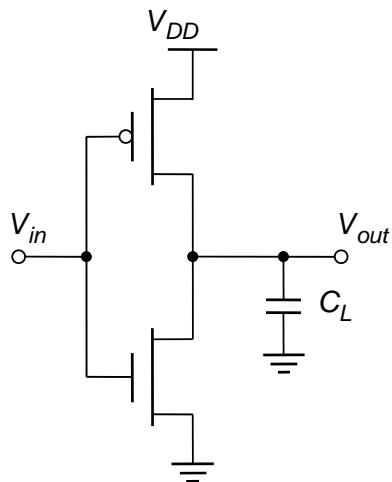
Switch Model (Width)

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CMOS Inverter Model



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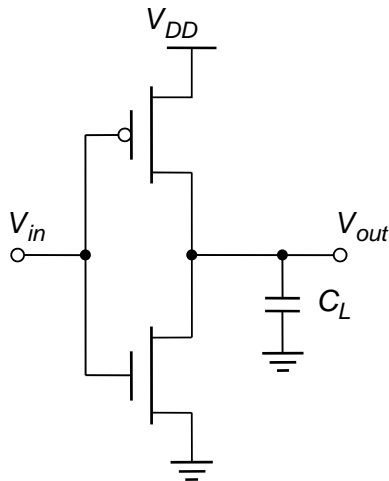
CMOS Logic

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The CMOS Inverter: A First Glance



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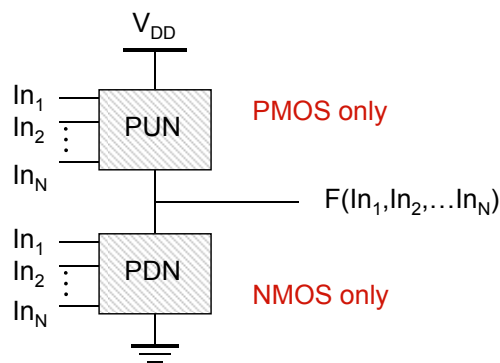
Static CMOS Gates

At every point in time (except during the switching transients) each **gate output is connected to either V_{DD} or V_{SS}** via a low resistive path.

The outputs of the gates **assume at all times the value of the Boolean function** implemented by the circuit (ignoring, once again, the transient effects during switching periods).

(Will contrast this later to **dynamic** circuit style.)

Static Complementary CMOS



PUN and PDN are **dual** logic networks
 PUN and PDN functions are **complementary**

Threshold Drops

PUN

PDN

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NMOS Transistors in Series/Parallel Connection

- Transistor \leftrightarrow switch controlled by its gate signal
 - NMOS switch on when switch control input is high

AND

$Y = X$ if **A AND B**

OR

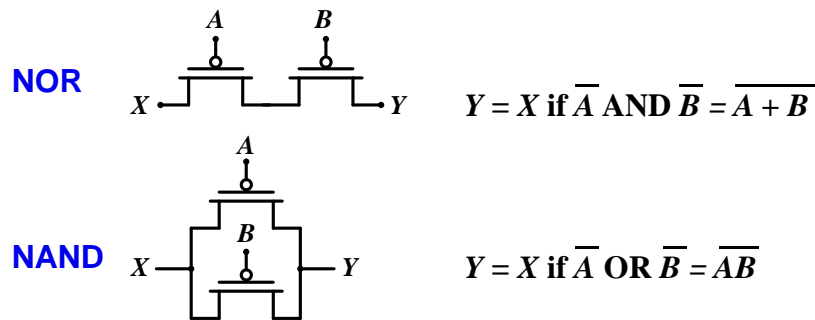
$Y = X$ if **A OR B**

- NMOS transistors pass a “strong” 0 but a “weak” 1

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PMOS Transistors in Series/Parallel Connection

- PMOS switch on when switch control is low



- PMOS transistors pass a “strong” 1 but a “weak” 0

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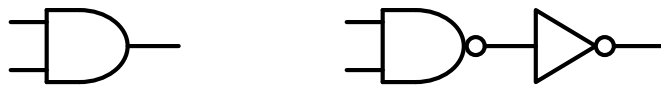
Complementary CMOS Logic Style

- PUP is the **dual** to PDN
(can be shown using DeMorgan's Theorems)

$$\overline{A + B} = \bar{A}\bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

- Static CMOS gates are always inverting



$$\text{AND} = \text{NAND} + \text{INV}$$

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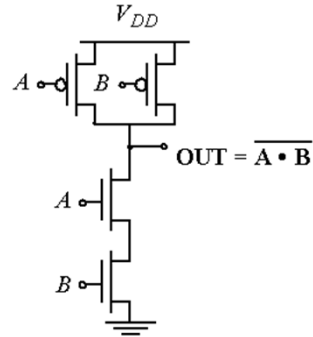
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Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

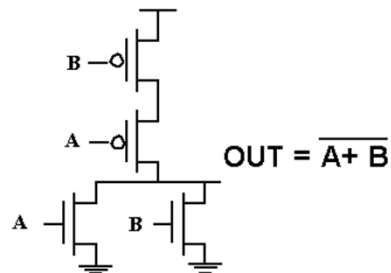


- PDN: $G = \overline{AB} \Rightarrow$ Conduction to GND
- PUN: $F = \overline{A + B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}
- $\overline{G(\ln_1, \ln_2, \ln_3, \dots)} \equiv F(\overline{\ln_1}, \overline{\ln_2}, \overline{\ln_3}, \dots)$

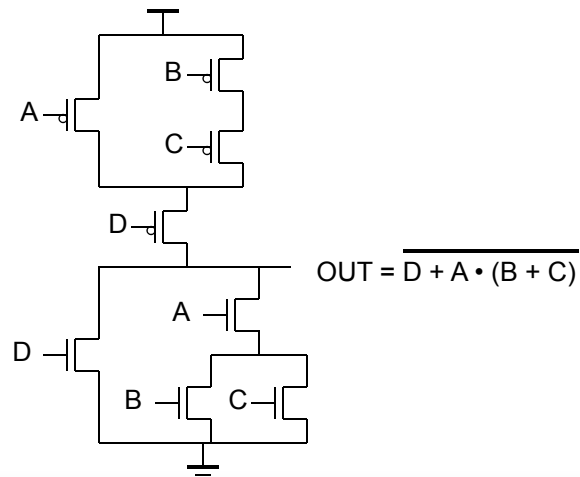
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



Complex CMOS Gate



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CMOS Properties

- Full rail-to-rail swing
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation

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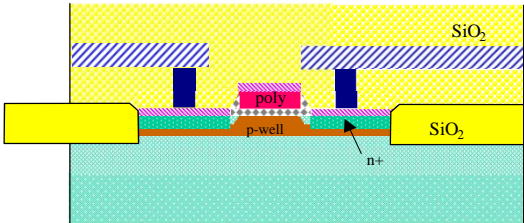


Design Rules

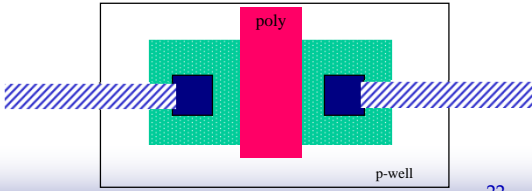
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Transistor Layout

Cross-Sectional View












Layout View





















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CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Well contact (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Layers in 0.25 μm CMOS process

Layer Description	Representation				
metal	 m1	 m2	 m3	 m4	 m5
well	 nw				
polysilicon	 poly				
contacts & vias	 ct	 v12,v23,v34,v45	 nwc	 pwc	
active area and FETs	 ndif	 pdif	 nfet	 pfet	
select (well contacts)	 nplus	 pplus	 prb		

Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
 - scalable design rules: lambda parameter
 - absolute dimensions (micron rules)

Design Rules

- Intra-layer
 - Widths, spacing, area
- Inter-layer
 - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25 μm)
 - Antenna rules, density rules, (area)

Intra-Layer Design Rules

The diagram illustrates design rules for various layers:

- Well:** Shows two yellow rectangles. For 'Same Potential', the spacing is 0 or 6, and the width is 10. For 'Different Potential', the spacing is 9.
- Active:** Shows two green rectangles with a spacing of 3 and a width of 3.
- Select:** Shows two dashed green rectangles with a spacing of 2.
- Polysilicon:** Shows two red rectangles with a spacing of 2 and a width of 2.
- Metal1:** Shows two blue rectangles with a spacing of 3 and a width of 3.
- Metal2:** Shows two magenta rectangles with a spacing of 4 and a width of 3.
- Contact or Via Hole:** Shows a black square with a width of 2 and a height of 2.

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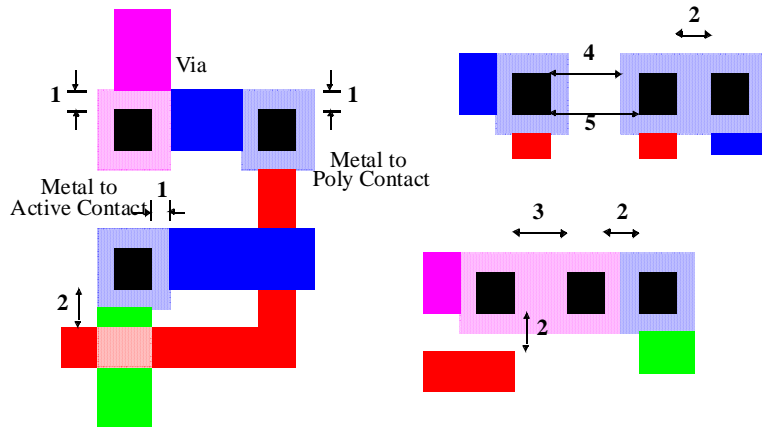
Inter-Layer: Transistor Layout

The diagram shows a transistor layout with the following dimensions:

- 1:** Thickness of the top metal layer.
- 2:** Width of the polysilicon gate.
- 3:** Width of the metal contact.
- 5:** Width of the well.

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Inter-Layer: Vias and Contacts

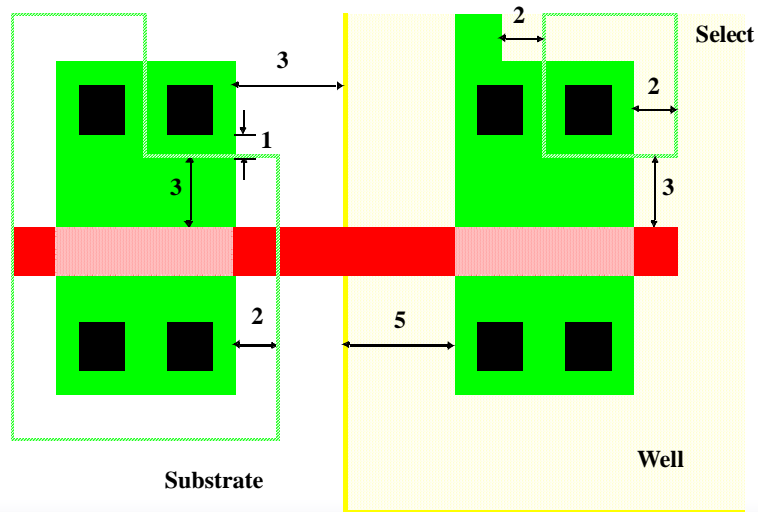


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Inter-Layer: Well and Substrate

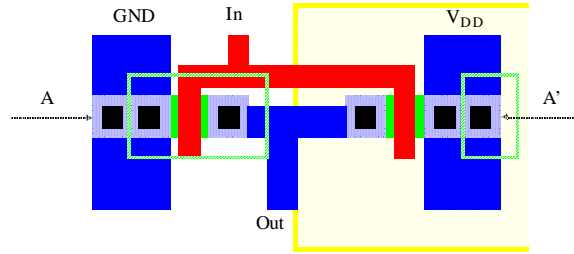


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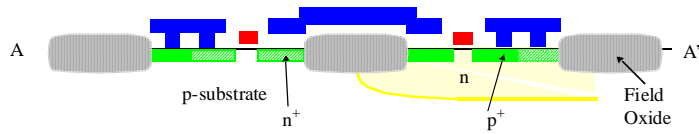
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CMOS Inverter Layout

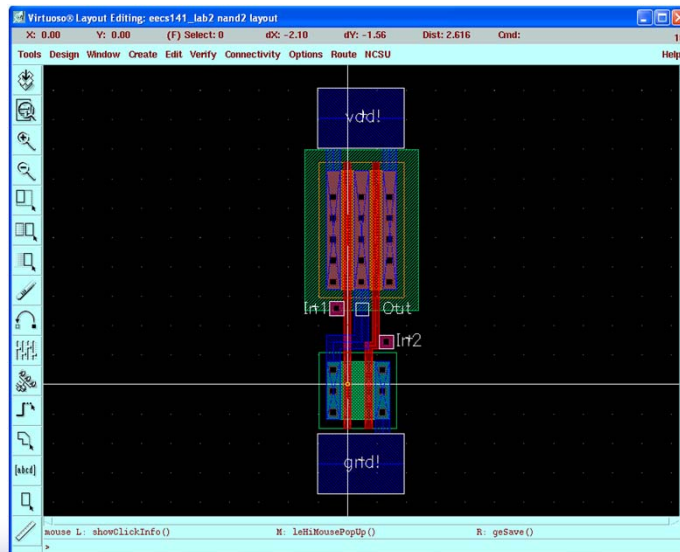


(a) Layout

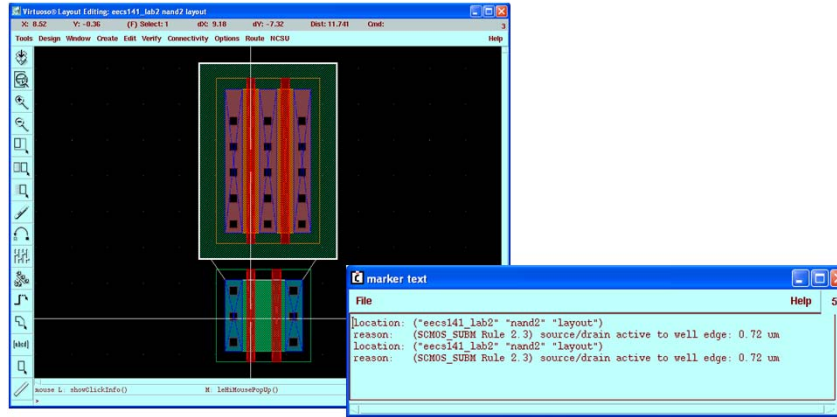


(b) Cross-Section along A-A'

Layout Editor



Design Rule Checker



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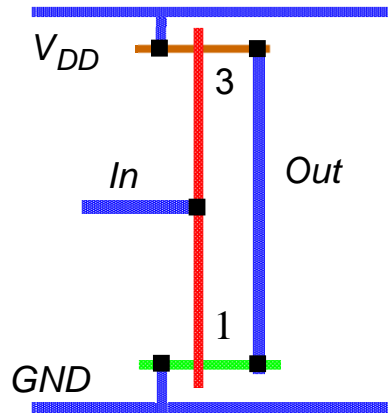
Layout vs. Schematic (LVS)

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Stick Diagram



- Dimensionless layout entities
- Only topology is important

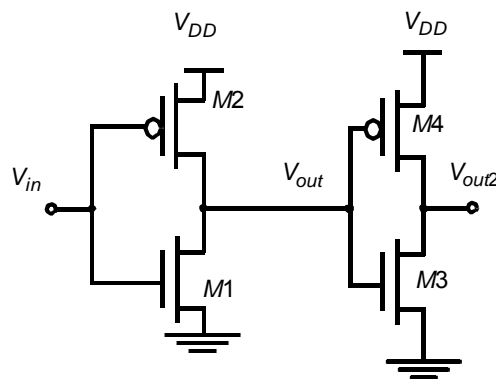
Stick diagram of inverter

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Circuit Under Design

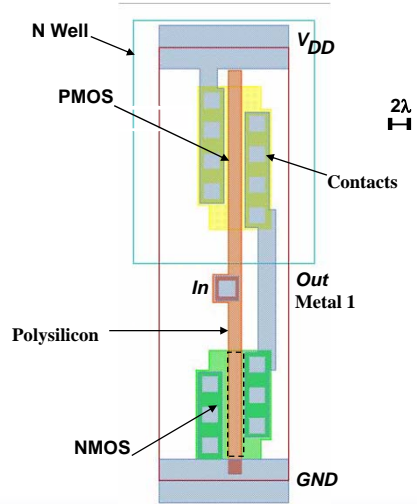
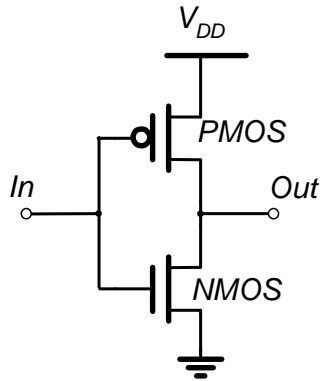


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CMOS Inverter



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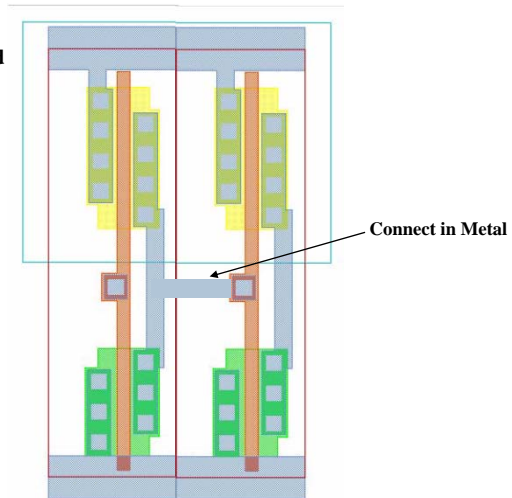
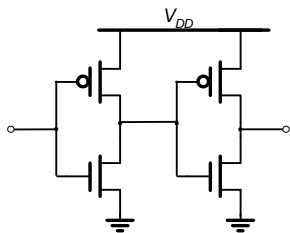
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Two Inverters

Share power and ground

Abut cells



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Next Lecture

- Overview of semiconductor memory