


*EE141-Fall 2012
Digital Integrated
Circuits*

Lecture 5
Overview of Semiconductor
Memory

EECS141 Lecture #5 1 ¹



*Semiconductor
Memory*

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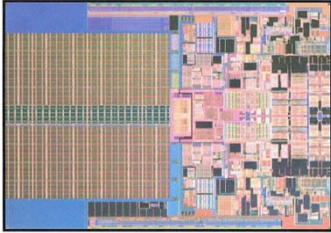
Announcements

- Homework #2 due today
- Homework #3 due next Thursday

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Why Memory?

Intel 45nm Core 2



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Class Material

- Last lecture
 - Detailed Switch Model
 - CMOS Gates
 - Design Rules
- Today's lecture
 - Overview of semiconductor memory
- Reading (Chapter 12.1, 12.2.3, 12.3.1)

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Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	Non-Random Access	EPROM E ² PROM	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM	FLASH	

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Random Access Memories (RAM)

□ STATIC (SRAM)

Data stored as long as supply is applied
Larger (6 transistors/cell)
Fast
Differential (usually)

□ DYNAMIC (DRAM)

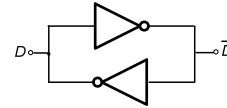
Periodic refresh required
Smaller (1-3 transistors/cell)
Slower
Single Ended

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Basic Static Memory Element



- If D is high, D_b will be driven low
- Which makes D stay high
- Positive feedback

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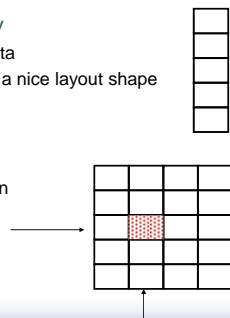
Random Access Chip Architecture

□ Conceptual: linear array

- Each box holds some data
- But this does not lead to a nice layout shape
- Too long and skinny

□ Create a 2-D array

- Decode Row and Column address to get data

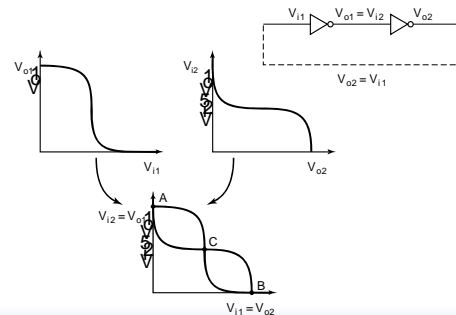


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Positive Feedback: Bi-Stability



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Basic Memory Array

CORE:

- keep square within a 2:1 ratio
- rows are **word lines**
- columns are **bit lines**
- data in and out on columns

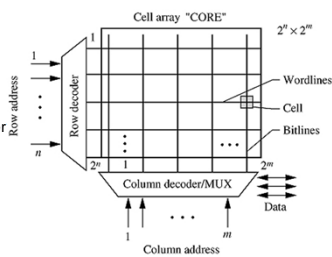
DECODERS:

- needed to reduce total number of pins; N+M address lines for 2^{N+M} bits of storage

Ex: if $N+M=20 \rightarrow 2^{20} = 1\text{Mb}$

MULTIPLEXING:

- used to select one or more columns for input or output of data

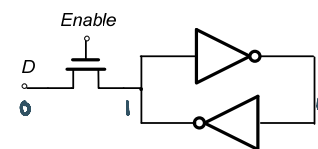


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Writing into a Cross-Coupled Pair



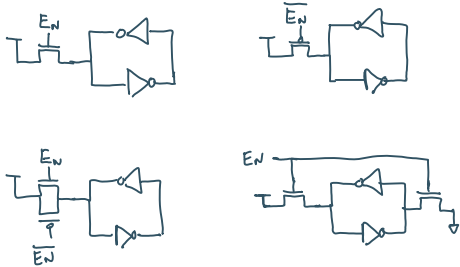
Access transistor must be able to overpower the feedback

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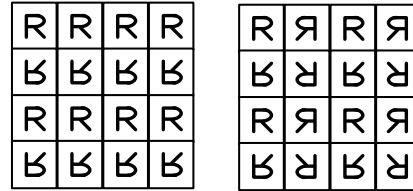
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Writing a "1"



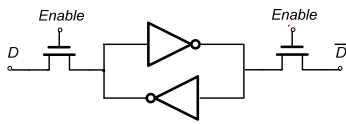
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SRAM Array Layout



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Memory Cell

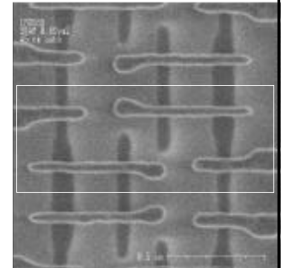
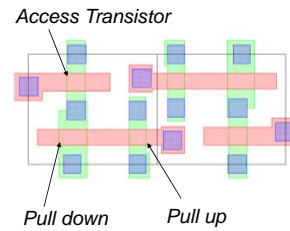


Complementary data values are written (read) from two sides

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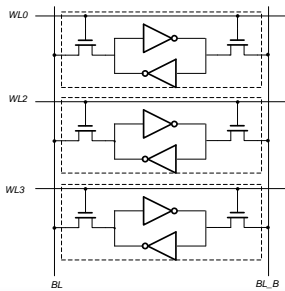
65nm SRAM

□ ST/Philips/Motorola



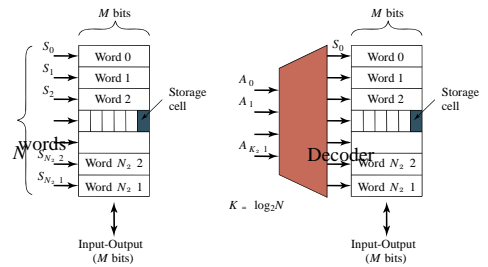
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SRAM Column



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Decoders



Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

Decoder reduces the number of select signals
 $K = \log_2 N$

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Row Decoders

Collection of 2^M complex logic gates
Organized in regular and dense fashion

(N)AND Decoder

$$WL_0 = \overline{A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9}$$

$$WL_{511} = A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$$

$WL_{16} =$

NOR Decoder

$$WL_0 = \overline{A_0 + A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 + A_8 + A_9}$$

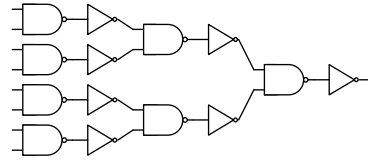
$$WL_{511} = \overline{A_0 + A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 + A_8 + A_9}$$

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Possible AND8



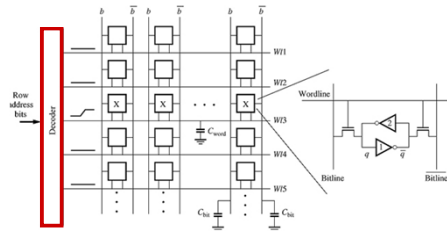
- Build 8-input NAND gate using 2-input gates and inverters
- Is this the best we can do?
- Is this better than using fewer NAND4 gates?

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Decoder Design Example



- Look at decoder for 256x256 memory block (8KBytes)

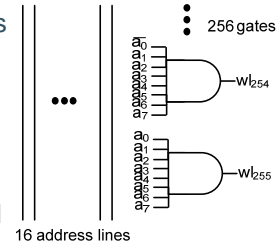
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Possible Decoder

- 256 8-input AND gates
 - Each built out of tree of NAND gates and inverters
- Need to drive a lot of capacitance (SRAM cells)
 - What's the best way to do this?



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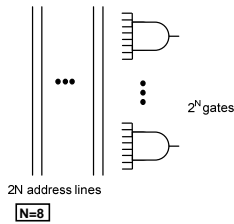
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Problem Setup

- Goal: Build fastest, lowest possible power decoder with static CMOS logic

- What we know

- Basically need 256 AND gates, each one of them drives one word line



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Next Lecture

- Buffer delay optimization

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