Inverter Chain

For some given $C_L$:
- How many stages are needed to minimize delay?
- How to size the inverters?

Anyone want to guess the solution?

Careful about Optimization Problems

- Get fastest delay if build one very big inverter
  - So big that delay is set only by self-loading

- Likely not the problem you’re interested in
  - Someone has to drive this inverter...

Engineering Optimization Problems in General

- Need to have a set of constraints

- Constraints key to:
  - Making the result useful
  - Making the problem have a 'clean' solution

- For sizing problem:
  - Need to constrain size of first inverter

Class Material

- Last lecture
  - Overview of Semiconductor Memory
- Today’s lecture
  - Inverter Delay Optimization
- Reading (5.4, 5.5)

Announcements

- Homework #3 due Thursday
- Homework #4 due next Thursday
Delay Optimization Problem #1

- You are given:
  - A fixed number of inverters
  - The size of the first inverter
  - The size of the load that needs to be driven

- Your goal:
  - Minimize the delay of the inverter chain

- Need model for inverter delay vs. size
  - But first, a simple example...

Simple Example: Two Inverters

\[ t_{\text{inv}} = 3 \cdot \ln(2) \cdot L \cdot R_{\text{sq}} C_{\text{g}} \]

Inverter Delay

- Minimum length devices, \( L = 0.09 \mu m \)
- Assume that for \( W_p = 2W_h = 2W \)
  - approximately equal resistances, \( R_p = R_h \)
  - approx. equal rise and fall delays, \( t_{\text{rise}} = t_{\text{fall}} \)

- Analyze as an RC network:
  \[ R_p = R_{\text{sq}} \left( \frac{L}{W_p} \right) = R_h = R_{\text{sq}} \left( \frac{L}{W_h} \right) = R_w \]

- Delay:
  \[ t_{\text{delay}} = t_{\text{rise}} = t_{\text{fall}} = (\ln 2) \cdot R_w C_{\text{int}} \]

Loading on the previous stage:
\[ C_{\text{in}} = 3WC_g \]

Inverter with Load

- Delay formula:
\[ t_{\text{inv}} = k R_p C_{\text{in}} \left( \frac{C_{\text{in}}}{C_{\text{int}}} + \frac{C_{\text{L}}}{C_{\text{in}}} \right) = t_{\text{inv}} (\gamma + f) \]

\[ C_{\text{in}} = \gamma C_{\text{in}} \] (\( \gamma = 1 \) for inverter)
\[ f = C_{\text{in}} / f_{\text{int}} \] - electrical fanout
\[ R_{\text{in}} = R_p L / W ; C_{\text{in}} = 3WC_g \]

- \( t_{\text{inv}} \) is independent of sizing of the gate!!!
Apply to Inverter Chain

\[ t_p = t_{p1} + t_{p2} + \ldots + t_{pN} \]

\[ t_{p1} = t_{sw}(y + \frac{C_{n,i+1}}{C_{i,n}}) \]

\[ t_p = \sum_{i=1}^{N} t_{sw}(y + \frac{C_{n,i+1}}{C_{i,n}}) \cdot C_{i,n+1} = C_L \]

Optimum Delay and Number of Stages

- When each stage has same fanout \( f \):
  \[ f^N = F = \frac{C_L}{C_{n,1}} \]

- Effective fanout of each stage:
  \[ f = \sqrt[2]{F} \]

- Minimum path delay:
  \[ t_p = N_t \left( y + \sqrt[2]{F} \right) \]

Optimal Tapering for Given \( N \)

- Delay equation has \( N-1 \) unknowns, \( C_{n,2}, \ldots, C_{n,N} \)

- To minimize the delay, find \( N-1 \) partial derivatives:
  \[ \frac{dt_p}{dC_{j,n-1}} = t_{sw} \cdot \left( \frac{1}{C_{j,n-1}} - \frac{1}{C_{j,n}} \right) \cdot C_{j,n+1} = 0 \]

Example

\[ C_1/C_1 \text{ has to be evenly distributed across } N = 3 \text{ stages:} \]

\[ f = \sqrt[3]{8} = 2 \]

Optimal Tapering for Given \( N \) (cont’d)

- Result: every stage has equal fanout:
  \[ \frac{C_{n,i+1}}{C_{i,n+1}} = \frac{C_{n,i}}{C_{i,n}} \]

- In other words, size of each stage is geometric mean of two neighbors:
  \[ C_{i,n} = \sqrt{C_{i,n-1} \cdot C_{i,n+1}} \]

- Equal fanout \( \rightarrow \) every stage will have same delay

Delay Optimization Problem #2

- You are given:
  - The size of the first inverter
  - The size of the load that needs to be driven

- Your goal:
  - Minimize delay by finding optimal number and sizes of gates

- So, need to find \( N \) that minimizes:
  \[ t_p = N_t \left( y + \sqrt[2]{F} \right) \]
**Intuitive Example**

\[ f^* = \frac{C_I}{C_n} \rightarrow N = \frac{\ln(C_I/C_n)}{\ln f} \]

\[ t_p = N \left( (C_I/C_n)^{1/3} + \gamma \right) = \frac{\ln(C_I/C_n)}{\ln f} \left( f + \gamma \right) \]

\[ \frac{\partial t_p}{\partial f} = \frac{\ln(C_I/C_n)}{\ln f} \cdot \frac{\ln^2 f - \ln f - \gamma/f}{f} = 0 \]

\[ f = \exp(1 + \gamma/f) \quad \text{For } \gamma = 0, f = e, \quad N = \ln(C_I/C_n) \]

**Solving the Optimization**

- Rewrite N in terms of fanout/stage \( f \):

**In Practice: Plot of Total Delay**

- Curves very flat for \( f > 2 \)
- Simplest/most common choice: \( f = 4 \)

**Normalized Delay As a Function of \( F \)**

\[ t_p = N \left( \gamma + \sqrt{F} \right), \quad F = C_I/C_n \]

**Optimum Effective Fanout \( f^* \)**

- Optimum \( f^* \) for given process defined by \( \gamma \)

\[ f = \exp(1 + \gamma/f) \]

- Intuition: why does \( f \) go up with \( \gamma \)?

**Buffer Design**

- Textbook page 250

- Simplest/most common choice: \( f = 4 \)

\[ N \quad f \quad t_p \]

<table>
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<th>( F )</th>
<th>Unbuffered</th>
<th>Two Stage</th>
<th>Inverter Chain</th>
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<td>8.5</td>
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<td>202</td>
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For \( \gamma = 1 \)
**What About Energy (and Area)?**

Ignoring diffusion capacitance:

\[ C_{\text{tot}} = C_i + f C_i + \ldots + f^N C_i \]

\[ = C_i \left( 1 + f + \ldots + f^N \right) \]

\[ = C_i + C_i f^{N+1} + C_i f \left( 1 + f + \ldots + f^N \right) \]

\[ = C_i \left( 1 + f + f^2 + \ldots + f^N \right) \]

\[ \text{Overhead } \approx \frac{f^{N+1}}{f-1} \]

**Example (N=0):**

- \( C_i = 20\text{pF} \)
- \( C_l = 50\text{fF} \)
- \( N = 6 \)

Fixed: \( 20\text{pF} \)

Overhead: \( 11.66\text{pF} \)

**Next Lecture**
- Gate Delay
- Logical Effort

**Example Overhead Numbers**

**Example:**

- \( C_i = 20\text{pF} \)
- \( C_l = 50\text{fF} \)

**Example Problem**