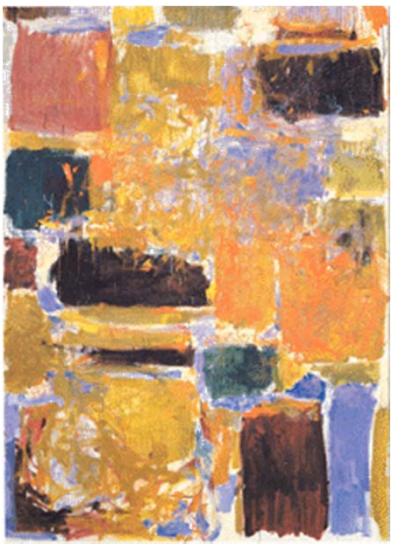


EE141-Fall 2012 Digital Integrated Circuits

Lecture 9
MOS Transistor Model

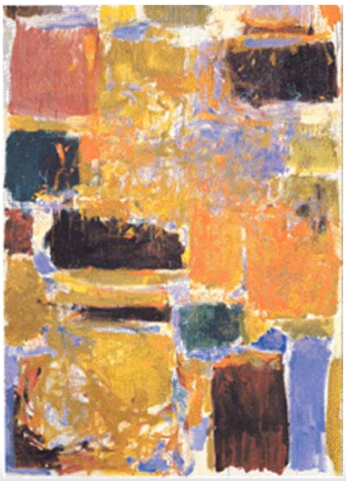
Announcements

- Homework #4 due today
- Homework #5 due next Thurs.
- Midterm #1 Thurs. Oct. 4th
  - Location TBA

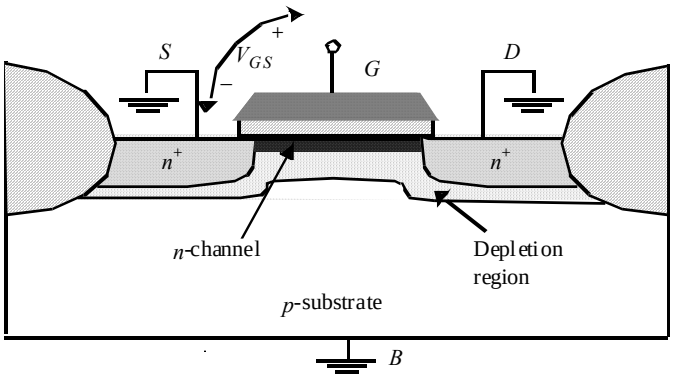
Class Material

- Last lecture
  - LE in decoders
- Today's lecture
  - MOS transistor modeling
    - Will see how to use these models to understand tradeoffs between CMOS gate delay, power, etc.
- Reading (3.3.1-3.3.2)

MOS Transistor



Threshold Voltage: Concept



- With positive gate bias, electrons pulled toward the gate
- With large enough bias, enough electrons will be pulled to "invert" the surface (p→n type)
- Voltage at which surface inverts: “magic” threshold voltage V_T

The Threshold Voltage

- Threshold

$$V_T = \varphi_{FB} + 2\varphi_F + \frac{Q_B}{C_{ox}}$$ ← Depletion charge

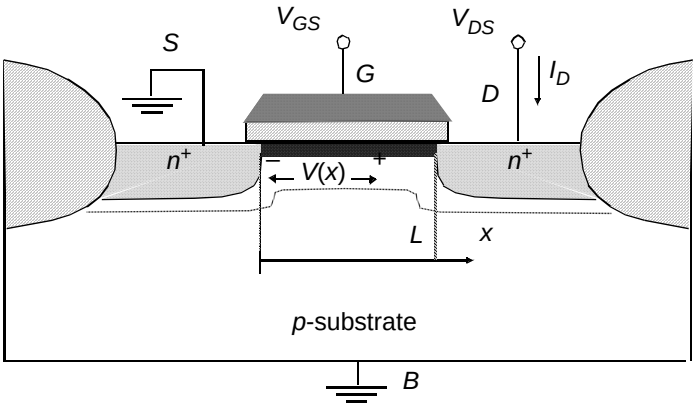
$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{2\varphi_F} \right)$$

- Fermi potential

$$\phi_F = \phi_T \cdot \ln \frac{N_A}{n_i}$$

$2\Phi_F$ is approximately 0.6V for p-type substrates
γ is the body factor
V_{T0} is approximately 0.45V for a 0.25um process

Transistor with Gate and Drain Bias



The Drain Current

- Charge density:

$$Q_i(x) =$$

- Velocity:

$$\upsilon_n(x) =$$

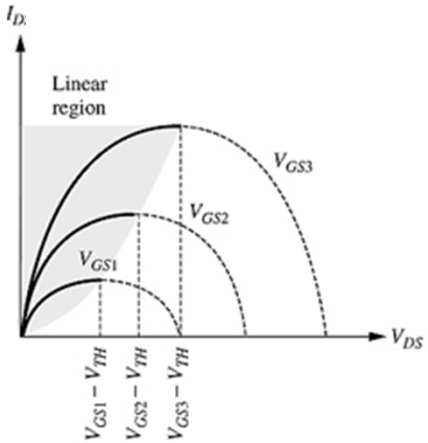
- Current:

$$I_D =$$

Solving the Drain Current

- Integrate along the channel:

Plot of I-V Curve



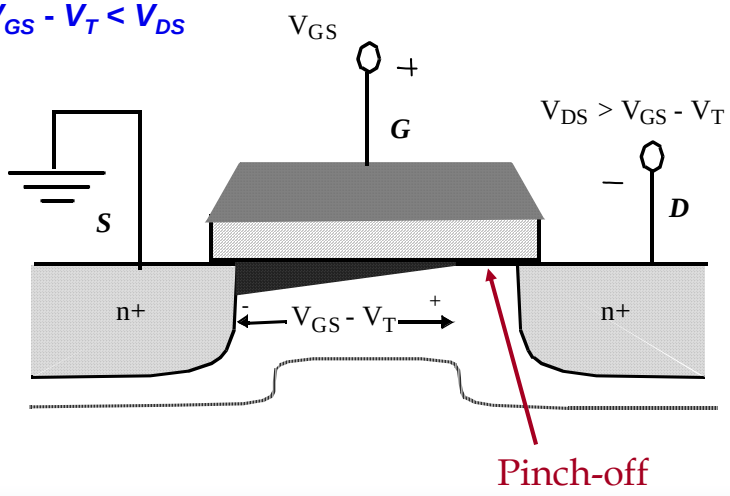
- Is this really what happens?

Cause of the Problem

- Why does the current bend down?
- When $(V_{GS}-V_{TH})-V_{DS}$ is negative, in our analysis the sign of the carriers changes
  - But transistors don't actually behave this way
- Look at what really happens to channel charge:

Transistor in Saturation

$0 < V_{GS} - V_T < V_{DS}$



Saturation

- For $(V_{GS} - V_T) < V_{DS}$, the effective drain voltage and current saturate:

$$V_{DS,eff} = (V_{GS} - V_T)$$

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

- Of course, real drain current isn't totally independent of V_{DS}
  - For example, approx. for channel-length modulation:

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

Modes of Operation

Cutoff:

$V_{GS} - V_T < 0$ $\quad I_D = 0$

Linear (Resistive):

$V_{GS} - V_T > V_{DS}$ $\quad I_D = k_n' \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$

Saturation:

$0 < V_{GS} - V_T < V_{DS}$ $\quad I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$

Another Way of Looking at This

Cutoff:

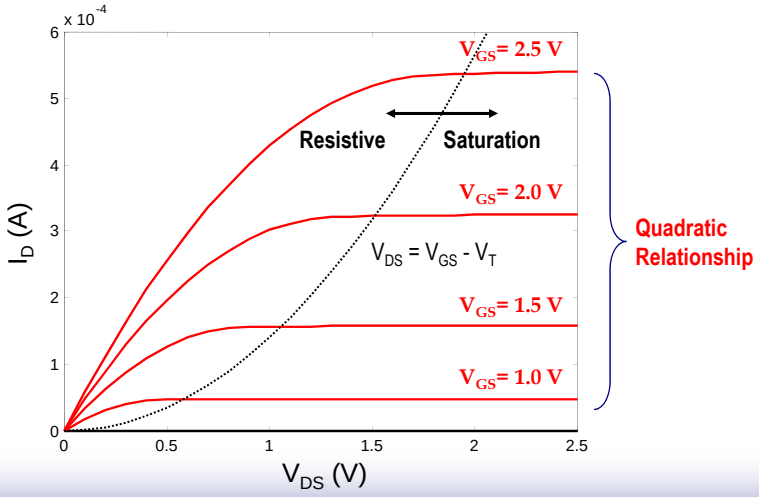
$V_{GS} - V_T < 0$ $\qquad I_D = 0$

On: (Linear or Saturated)

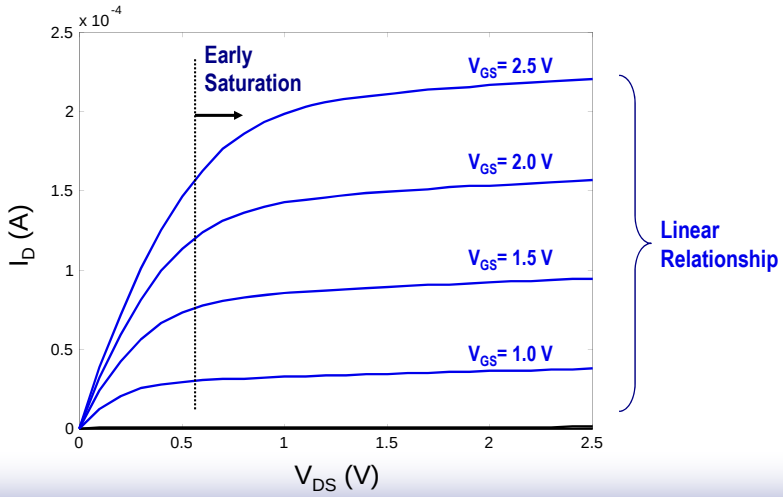
$V_{DS,eff} = \min(V_{GS} - V_T, V_{DS})$

$$I_D = k_n \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS,eff} - \frac{V_{DS,eff}^2}{2} \right]$$

Current-Voltage Relations: A Good Ol' Transistor

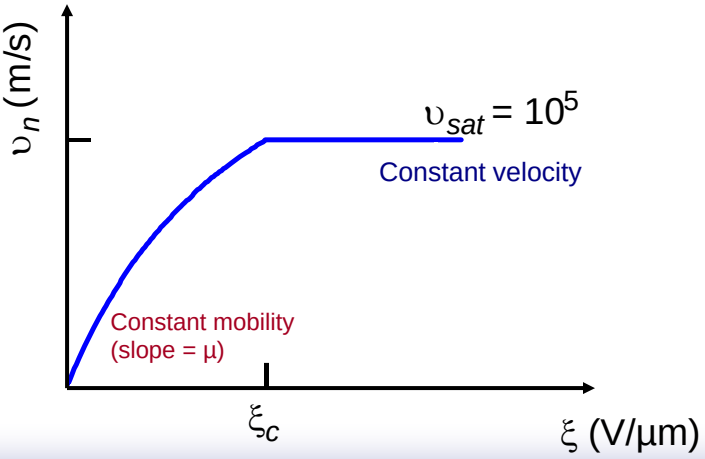


Current-Voltage Relations: The Deep Sub-Micron Transistor

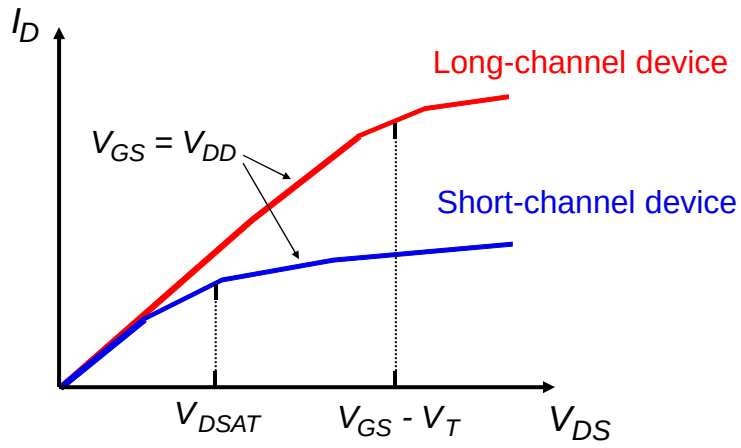


Velocity Saturation

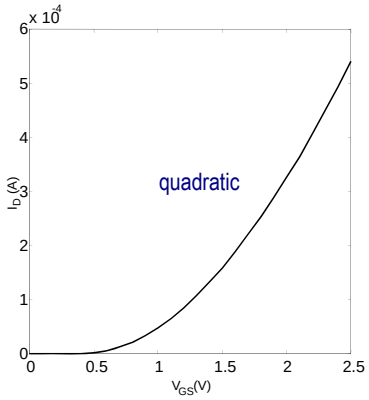
- Velocity saturates due to carrier scattering effects



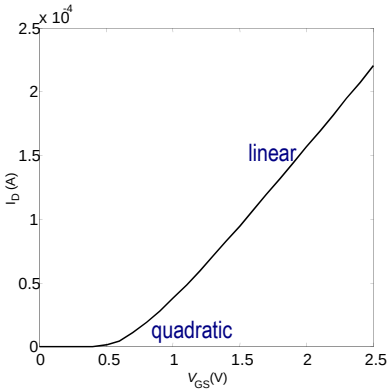
Velocity Saturation



I_D versus V_{GS}



Long Channel
(L=2.5μm)



Short Channel
(L=0.25μm)

Including Velocity Saturation

Approximate velocity:

$$\upsilon = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \le \xi_c$$

$$= \upsilon_{sat} \quad \text{for} \quad \xi \ge \xi_c$$

Continuity requires that:

$$\xi_c = 2\upsilon_{sat}/\mu_n$$

Integrating to find the current again:

$$I_D = \frac{\mu_n C_{ox}}{1 + (V_{DS}/\xi_c L)}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Velocity Saturation Drain Current

- Saturation occurs when carriers reach υ_{sat}

$$I_D = WC_{ox}(V_{GS} - V_T - V_{DSAT})\upsilon_{sat}$$

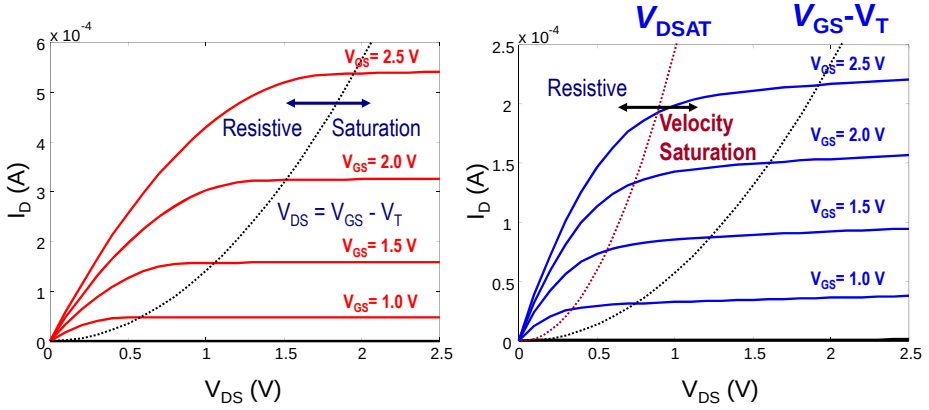
- We also know that:

$$I_D = \frac{\mu_n C_{ox}}{1 + (V_{DSAT}/\xi_c L)}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

- Equating the two expressions gives V_{DSAT} and I_D:

$$V_{DSAT} = \frac{(V_{GS} - V_T)\xi_c L}{(V_{GS} - V_T) + \xi_c L} \qquad I_D = W\upsilon_{sat}C_{ox}\frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + \xi_c L}$$

Regions of Operation



Long Channel (L=2.5μm)

W/L=1.5

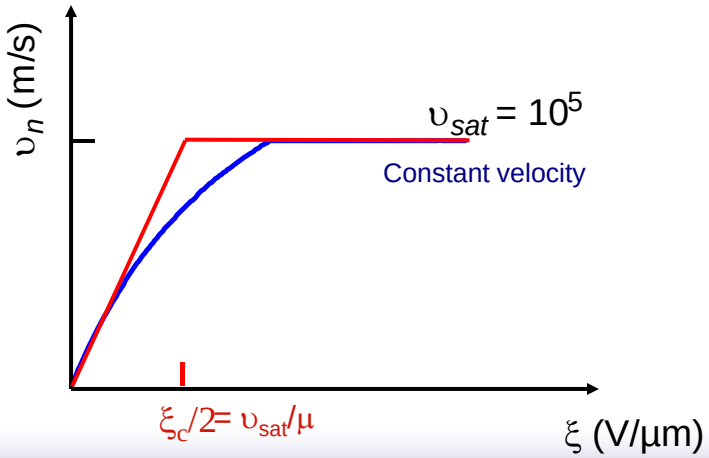
Short Channel (L=0.25μm)

Models, Models, Models…

- Exact behavior of transistor in velocity sat. somewhat challenging if want simple/easy to use models
- So, many different models developed over the years
  - v-sat, alpha, unified, V_T*, etc.
- I often use v-sat model I just presented
  - Works well for calculating LE of complex gates (more later)
  - But still somewhat complicated – often want even simpler model

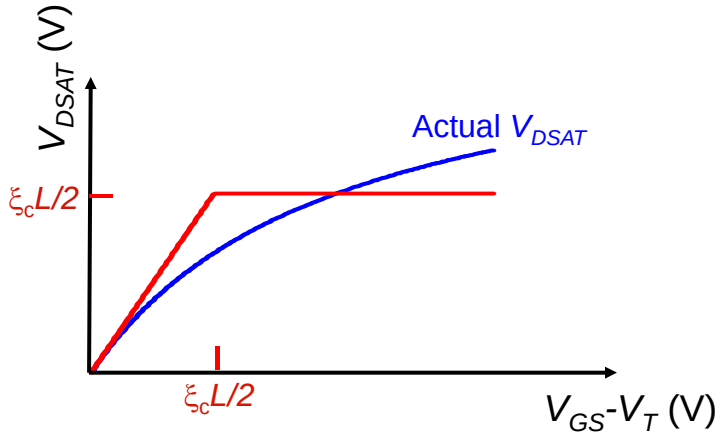
Simplified Velocity Saturation

- Assume velocity perfectly linear until hit υ_{sat}



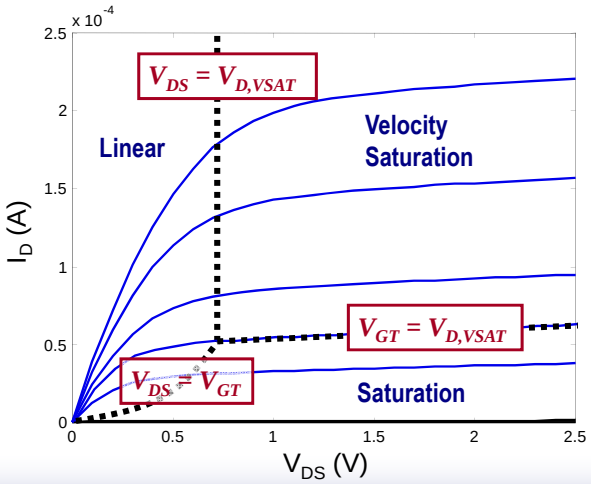
Simplified Velocity Saturation *(cont'd)*

- Assume $V_{DSAT} = \xi_c L/2$ when $(V_{GS} - V_T) > \xi_c L/2$



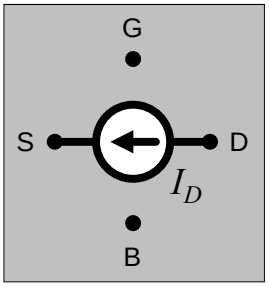
Simplified Model

- Define $V_{GT} = V_{GS} - V_T$, $V_{D,VSAT} = \xi_c \cdot L/2$



A Unified Model for Manual Analysis

define $V_{GT} = V_{GS} - V_T$



for $V_{GT} \leq 0$: $I_D = 0$

for $V_{GT} \geq 0$:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{DS,eff} - \frac{V_{DS,eff}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

with $V_{DS,eff} = \min (V_{GT}, V_{DS}, V_{D,VSAT})$

One Last Simplification

- If device always operates in velocity sat.:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{D,VSAT}}{2} \right) V_{D,VSAT}$$

- "V_T*" model:

$$V_T^* \equiv V_T + \frac{V_{D,VSAT}}{2}$$

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T^* \right) V_{D,VSAT}$$

- Good for first cut, simple analysis

Next Lecture

- Using the MOS model: VTCs