Announcements

- Homework #4 due today
- Homework #5 due next Thurs.
- Midterm #1 Thurs. Oct. 4th
  - Location TBA

Class Material

- Last lecture
  - LE in decoders
- Today’s lecture
  - MOS transistor modeling
    - Will see how to use these models to understand tradeoffs between CMOS gate delay, power, etc.
- Reading (3.3.1-3.3.2)

Threshold Voltage: Concept

- With positive gate bias, electrons pulled toward the gate
- With large enough bias, enough electrons will be pulled to "invert" the surface (p→n type)
- Voltage at which surface inverts: “magic” threshold voltage $V_T$

The Threshold Voltage

- Threshold
  $$V_T = \phi_F + 2\phi_F \frac{Q}{C_{ox}}$$
  $$V_T = V_{gs} + \gamma \left( \frac{\sqrt{V_{gs} + V_{th,n}} - \sqrt{V_{gs}}}{\gamma} \right)$$

- Fermi potential
  $$\phi_F = \phi_F - \ln \frac{N_A}{n_i}$$
  $2\phi_F$ is approximately 0.6V for p-type substrates
  $\gamma$ is the body factor
  $V_{th,n}$ is approximately 0.45V for a 0.25um process
The Drain Current

- Charge density:
  \[ Q(x) = \]

- Velocity:
  \[ u_n(x) = \]

- Current:
  \[ I_D = \]

Cause of the Problem

- Why does the current bend down?

- When \((V_{GS} - V_{TH}) - V_{DS}\) is negative, in our analysis the sign of the carriers changes.
  - But transistors don’t actually behave this way.

- Look at what really happens to channel charge:

Solving the Drain Current

- Integrate along the channel:

Transistor in Saturation

\(0 < V_{GS} - V_T < V_{DS}\)
Saturation

- For \((V_{GS} - V_t) < V_{DS}\), the effective drain voltage and current saturate:

\[
V_{DS,\text{eff}} = (V_{GS} - V_t)
\]

\[
I_D = \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2
\]

- Of course, real drain current isn’t totally independent of \(V_{DS}\)
  - For example, approx. for channel-length modulation:

\[
I_D = \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda \cdot V_{DS})
\]

Modes of Operation

Cutoff:

- \(V_{GS} - V_t < 0\)  
  \(I_D = 0\)

Linear (Resistive):

- \(V_{GS} - V_t > V_{DS}\)  
  \(I_D = k_n \frac{W}{L} \left( (V_{GS} - V_t) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)\)

Saturation:

- \(0 < V_{GS} - V_t < V_{DS}\)  
  \(I_D = \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda \cdot V_{DS})\)

Another Way of Looking at This

Cutoff:

- \(V_{GS} - V_t < 0\)  
  \(I_D = 0\)

On: (Linear or Saturated)

- \(V_{DS,\text{eff}} = \min(V_{GS} - V_t, V_{DS})\)  
  \(I_D = \frac{k_n}{2L} \left( (V_{GS} - V_t) \cdot V_{DS,\text{eff}} - \frac{V_{DS,\text{eff}}^2}{2} \right)\)

Current-Voltage Relations: A Good Ol’ Transistor

Current-Voltage Relations: The Deep Sub-Micron Transistor

Velocity Saturation

- Velocity saturates due to carrier scattering effects

\[
\nu_{\text{sat}} = 10^5 \text{ m/s}
\]

Constant velocity

\[
\xi = \text{V}{/\mu\text{m}}
\]
**Velocity Saturation**

- **Long-channel device**
- **Short-channel device**

**Velocity Saturation Drain Current**

- Saturation occurs when carriers reach $v_{sat}$
  
  \[ I_D = W C_s (V_{GS} - V_T) \frac{V_{DS} - V_T}{V_{DSAT}} \]

- We also know that:
  
  \[ I_D = \mu C_s (V_{GS} - V_T) \frac{V_{DS}^2}{L} \]

- Equating the two expressions gives $V_{DSAT}$ and $I_D$:
  
  \[ V_{DSAT} = \frac{(V_{GS} - V_T) L}{(V_{GS} - V_T + \xi L)} \]

  \[ I_D = \frac{W D_s C_s (V_{GS} - V_T)^2}{(V_{GS} - V_T + \xi L)} \]

**$I_D$ versus $V_{GS}$**

- **Long Channel** (L=2.5\(\mu\)m)
- **Short Channel** (L=0.25\(\mu\)m)

**Regions of Operation**

- **Long Channel** (L=2.5\(\mu\)m) W/L=1.5
- **Short Channel** (L=0.25\(\mu\)m)

**Including Velocity Saturation**

- Approximate velocity:
  \[ u = \frac{\xi}{2 \xi_{sat} / \mu} \text{ for } \xi \leq \xi_{sat} \]

- Continuity requires that:
  \[ \xi_{sat} = 2 \xi_{sat} / \mu \]

- Integrating to find the current again:
  \[ I_D = \frac{W C_s}{1 + (V_{DSAT} / \xi L)} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

**Models, Models, Models...**

- Exact behavior of transistor in velocity sat. somewhat challenging if want simple/easy to use models

- So, many different models developed over the years
  - \(v\)-sat, alpha, unified, \(V_{f*}\), etc.

- I often use \(v\)-sat model I just presented
  - Works well for calculating LE of complex gates (more later)
  - But still somewhat complicated – often want even simpler model
Simplified Velocity Saturation

- Assume velocity perfectly linear until hit \( v_{\text{sat}} \)

\[
v_{\text{sat}} = \frac{10^6}{\mu m}
\]

Constant velocity

\[
\xi = \frac{v_{\text{sat}}}{\mu m}
\]

Simplified Velocity Saturation (cont’d)

- Assume \( V_{\text{DSAT}} = \frac{\xi}{2} \) when \( (V_{GS} - V_T) > \frac{\xi}{2} \)

A Unified Model for Manual Analysis

Define \( V_{GT} = V_{GS} - V_T \)

- For \( V_{GT} \leq 0 \): \( I_D = 0 \)

- For \( V_{GT} \geq 0 \):
  \[
  I_D = k \cdot \frac{W}{L} \left( V_{GT} \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \left( 1 + \lambda \cdot V_{GS} \right)
  \]
  with \( V_{DSAT} = \min (V_{DS}, V_{GS}, V_{D,\text{SAT}}) \)

One Last Simplification

- If device always operates in velocity sat.:
  - "\( V_T^* \)" model:
    \[
    V_T^* = V_T + \frac{V_{DSAT}}{2}
    \]
    \[
    I_D = k \cdot \frac{W}{L} \left( V_{GT} - V_T^* \right) V_{D,\text{SAT}}
    \]
  - Good for first cut, simple analysis

Next Lecture

- Using the MOS model: VTCs