CMOS Manufacturing Process
CMOS Process
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS Process
This two-inverter circuit (of Figure 3.25 in the text) will be manufactured in a twin-well process.
Circuit Layout
The Manufacturing Process

For a great tour through the process and its different steps, check
http://www.fullman.com/semiconductors/semiconductors.html

For a complete walk-through of the process (64 steps), check the
Book web-page

http://bwrc.eecs.berkeley.edu/Classes/IcBook
Typical operations in a single photolithographic cycle (from [Fullman]).
Patterning of SiO₂

(a) Silicon base material

(b) After oxidation and deposition of negative photoresist

(c) Stepper exposure

UV-light
Patterned optical mask
Exposed resist

(d) After development and etching of resist, chemical or plasma etch of SiO₂

(e) After etching

(f) Final result after removal of resist
CMOS Process at a Glance

- Define active areas
- Etch and fill trenches
- Implant well regions
- Deposit and pattern polysilicon layer
- Implant source and drain regions and substrate contacts
- Create contact and via windows
- Deposit and pattern metal layers
CMOS Process Walk-Through

(a) Base material: p+ substrate with p-epi layer

(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask
CMOS Process Walk-Through

(d) After trench filling, CMP planarization, and removal of sacrificial nitride

(e) After n-well and $V_{Tp}$ adjust implants

(f) After p-well and $V_{Tn}$ adjust implants
CMOS Process Walk-Through

(g) After polysilicon deposition and etch

(h) After \( n^+ \) source/drain and \( p^+ \) source/drain implants. These steps also dope the polysilicon.

(i) After deposition of \( \text{SiO}_2 \) insulator and contact hole etch.
CMOS Process Walk-Through

(j) After deposition and patterning of first Al layer.

(k) After deposition of SiO$_2$ insulator, etching of via’s, deposition and patterning of second layer of Al.
Advanced Metalization
Advanced Metalization

Dual damascene IC process

- Oxide deposition
- Stud lithography and reactive ion etch
- Wire lithography and reactive ion etch
- Stud and wire metal deposition
- Metal chemical-mechanical polish

Source: IBM Corp.
Design Rules

Jan M. Rabaey
3D Perspective
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  » scalable design rules: lambda parameter
  » absolute dimensions (micron rules)
## CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td>![Yellow]</td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td>![Green]</td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td>![Green]</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td>![Red]</td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td>![Blue]</td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td>![Magenta]</td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td>![Black]</td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td>![Black]</td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td>![Black]</td>
</tr>
</tbody>
</table>
Layers in 0.25 µm CMOS process

<table>
<thead>
<tr>
<th>Layer Description</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>m1 m2 m3 m4 m5</td>
</tr>
<tr>
<td>well</td>
<td>nw</td>
</tr>
<tr>
<td>polysilicon</td>
<td>poly</td>
</tr>
<tr>
<td>contacts &amp; vias</td>
<td>ct v12,v23,v34,v45</td>
</tr>
<tr>
<td>active area and FETs</td>
<td>ndif pdif nfct pfcet</td>
</tr>
<tr>
<td>select</td>
<td>nplus pplus prb</td>
</tr>
</tbody>
</table>
Intra-Layer Design Rules

- **Well**: Same Potential (0 or 6) and Different Potential (9).
- **Active**: 3 units of separation.
- **Select**: 2 units of separation.
- **Contact or Via Hole**: 2 units of separation.
- **Polysilicon**: 2 units of separation.
- **Metal1**: 3 units of separation.
- **Metal2**: 4 units of separation.
Transistor Layout
Vias and Contacts

1. Via
2. Metal to Active Contact
3. Metal to Poly Contact
4. 4
5. 5
Select Layer

Substrate

Well

Select
CMOS Inverter Layout

(a) Layout

(b) Cross-Section along A-A’
Layout Editor
Design Rule Checker

poly_not_fet to all_diff minimum spacing = 0.14 um.
Sticks Diagram

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

Stick diagram of inverter