

EE141- Spring 2003

Lecture 4

Design Rules
CMOS Inverter
MOS Transistor Model



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Today's lecture

- Design Rules
- The CMOS inverter at a glance
- An MOS transistor model for manual analysis

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Important!

- Labs start next week
- You must show up in one of the lab sessions next week
- If you don't show up you will be dropped from the class
 - » Unless you let me know that you still want to be in the class
- Homework 2 will be posted later today. Due next Thursday, February 6.

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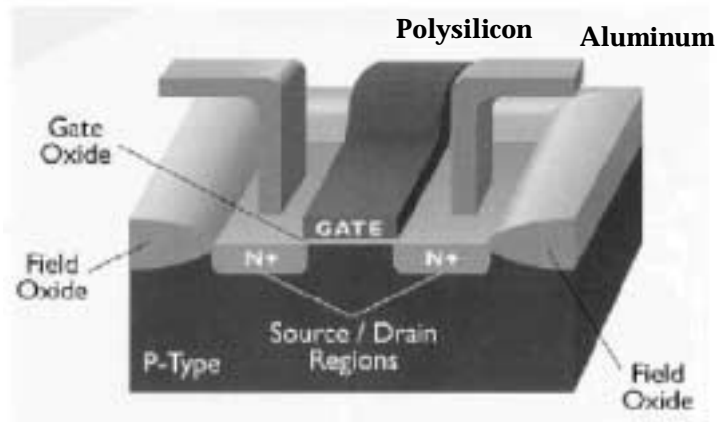
Design Rules

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3D Perspective












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Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
 - » scalable design rules: lambda parameter
 - » absolute dimensions (micron rules)




















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CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

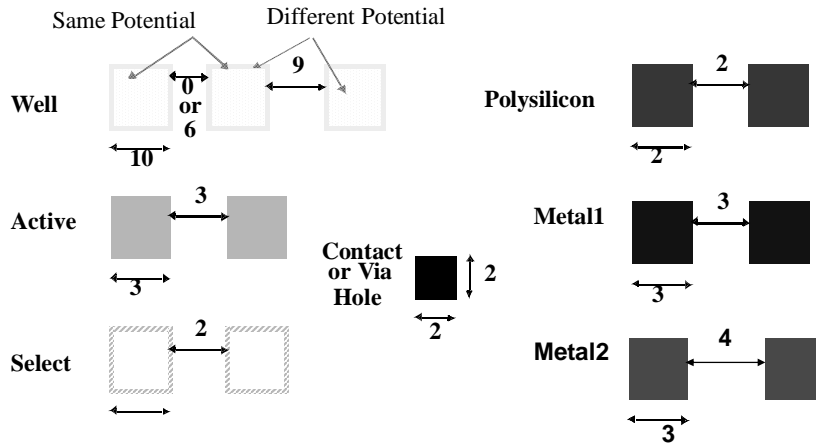
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Layers in 0.25 μm CMOS process

Layer Description	Representation				
metal	 m1	 m2	 m3	 m4	 m5
well	 w0				
polysilicon	 poly				
contacts & vias	 c1	 c2, c3, c4, c5	 c3	 c4	 c5
active areas and FEFs	 a1	 a2	 a3	 a4	
select	 s1	 s2	 s3		

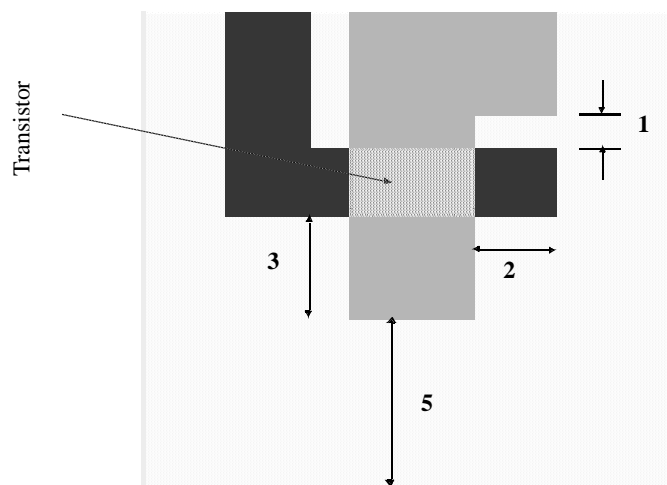
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Intra-Layer Design Rules



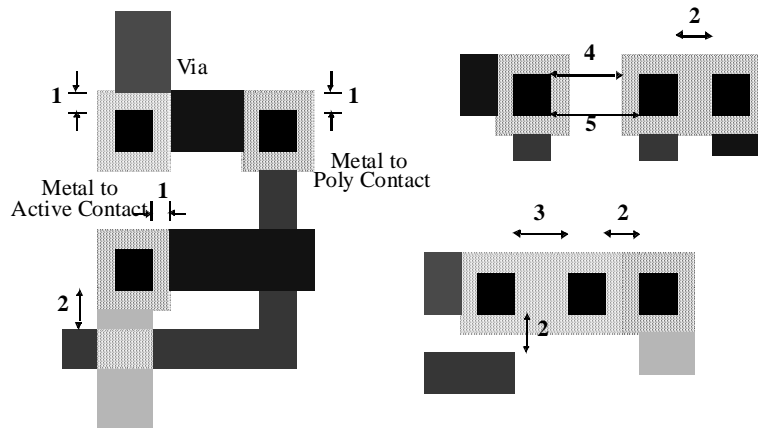
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Transistor Layout



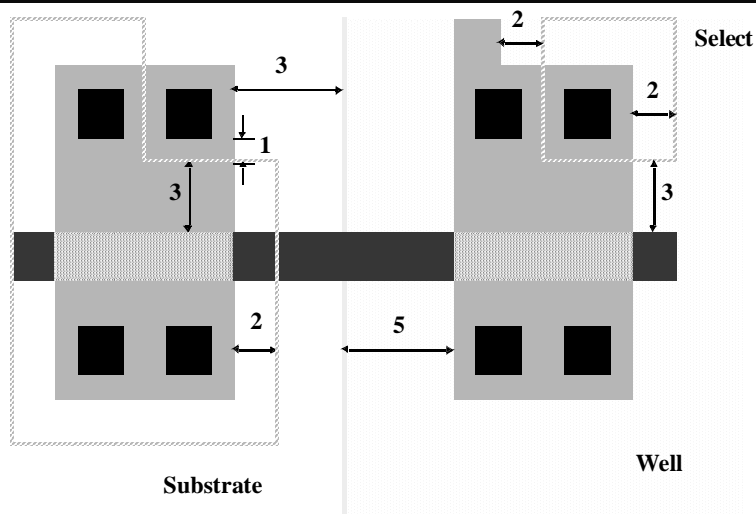
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Vias and Contacts



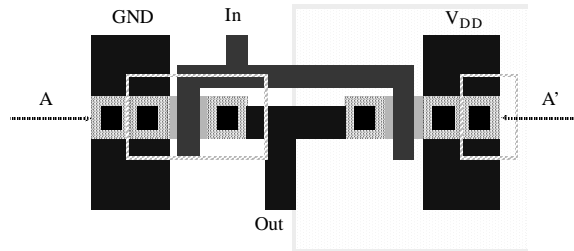
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Select Layer

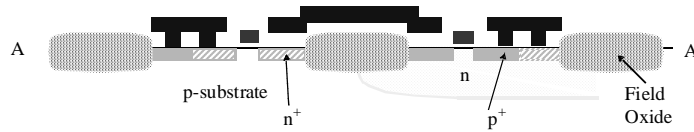


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CMOS Inverter Layout



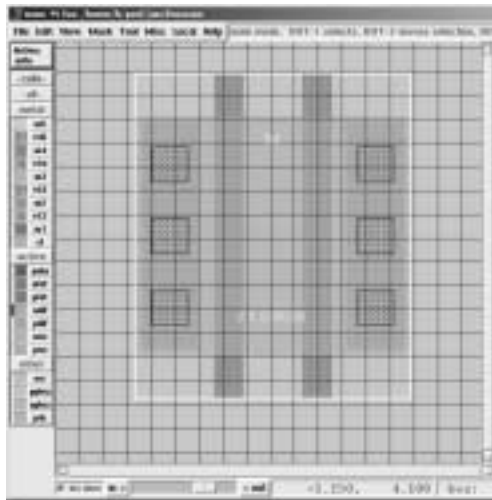
(a) Layout



(b) Cross-Section along A-A'

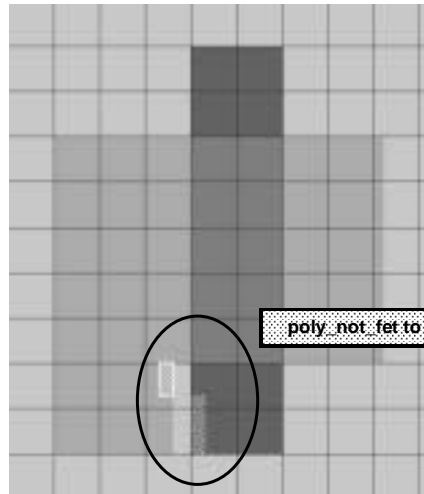
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Layout Editor



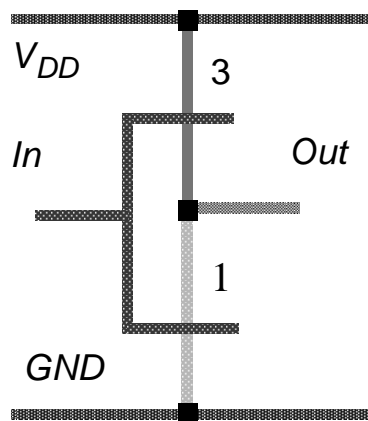
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Design Rule Checker



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Sticks Diagram



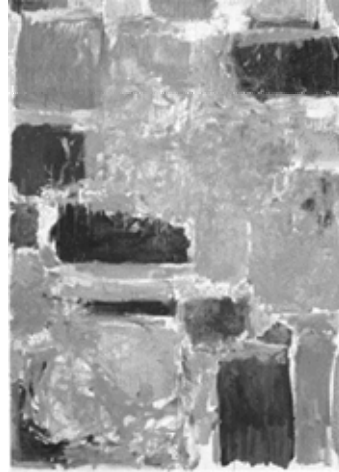
- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

Stick diagram of inverter

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CMOS Inverter MOS Transistor

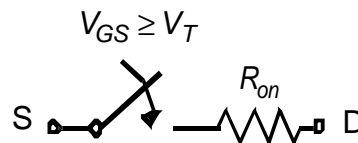
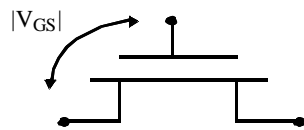
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What is a Transistor?

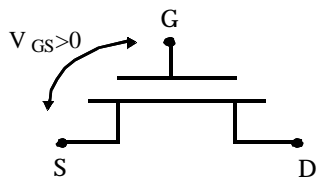
A MOS Transistor \longleftrightarrow A Switch!



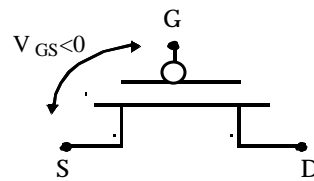
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NMOS and PMOS

NMOS Transistor

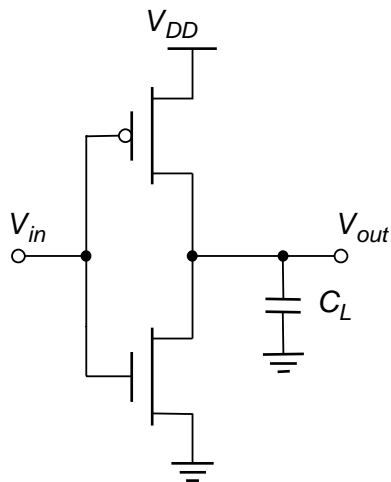


PMOS Transistor



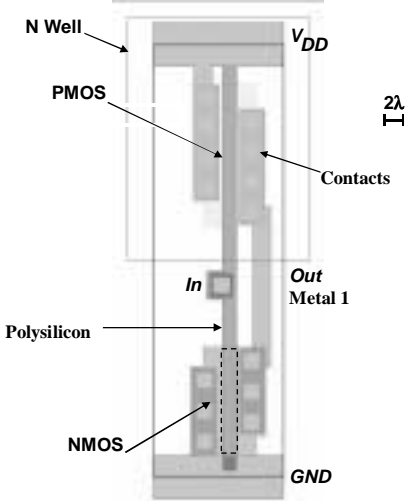
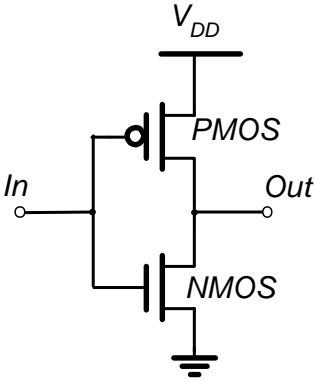
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The CMOS Inverter: A First Glance



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CMOS Inverter

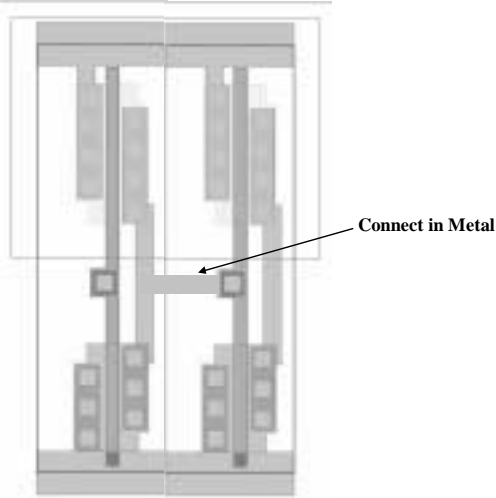
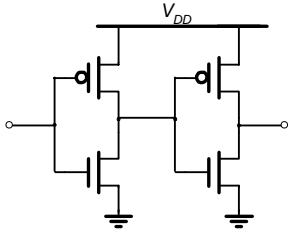


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Two Inverters

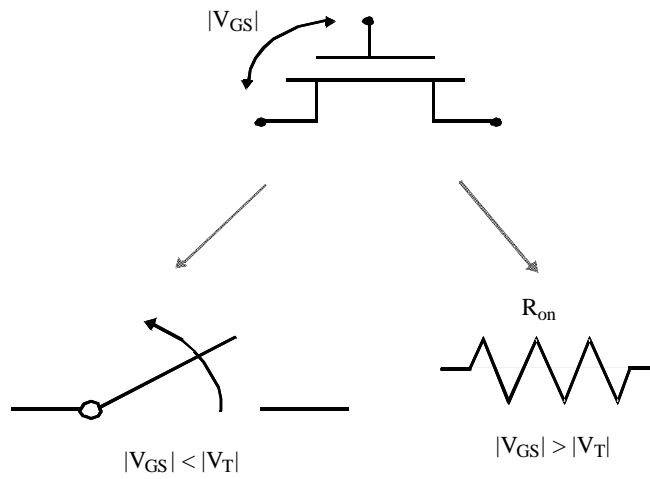
Share power and ground

Abut cells



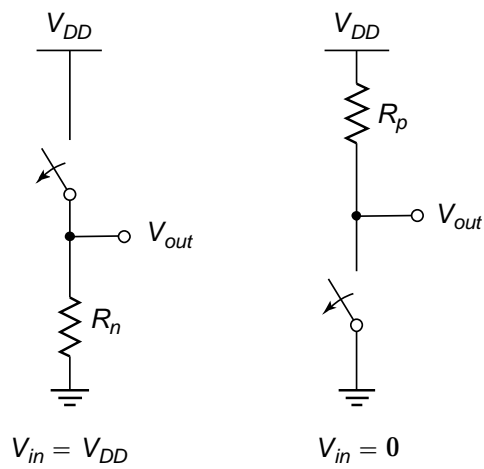
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Switch Model of CMOS Transistor



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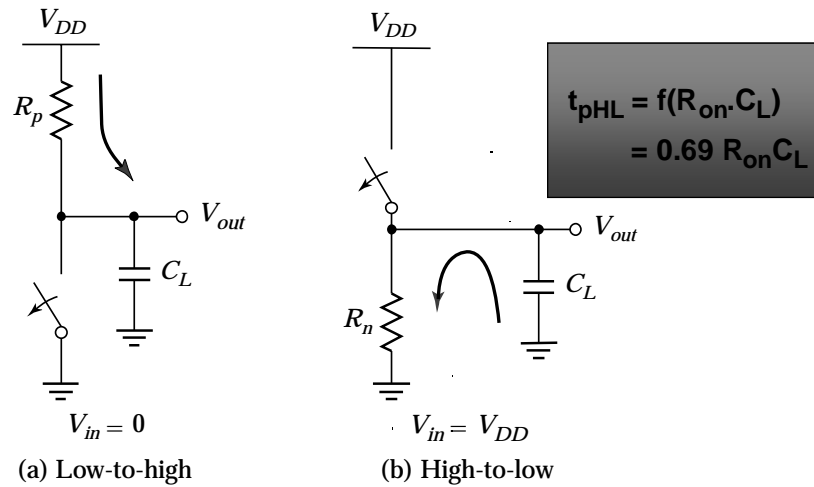
CMOS Inverter First-Order DC Analysis



$$\begin{aligned}
 V_{OL} &= 0 \\
 V_{OH} &= V_{DD} \\
 V_M &= f(R_n, R_p)
 \end{aligned}$$

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CMOS Inverter: Transient Response



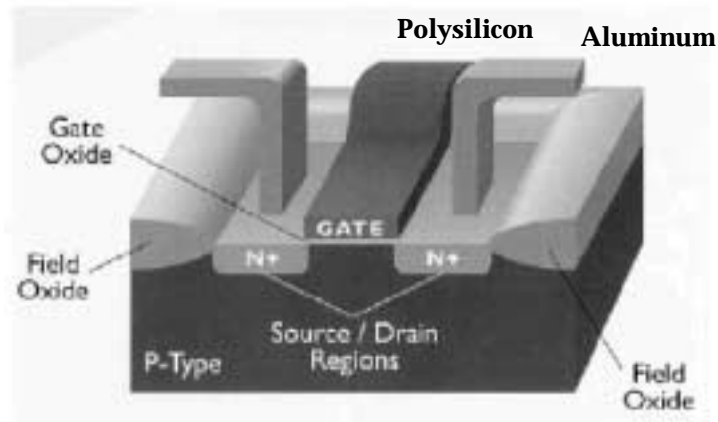
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CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

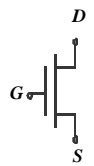
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The MOS Transistor

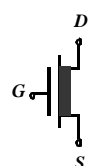


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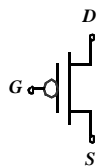
MOS Transistors - Types and Symbols



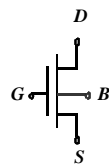
NMOS Enhancement



NMOS Depletion



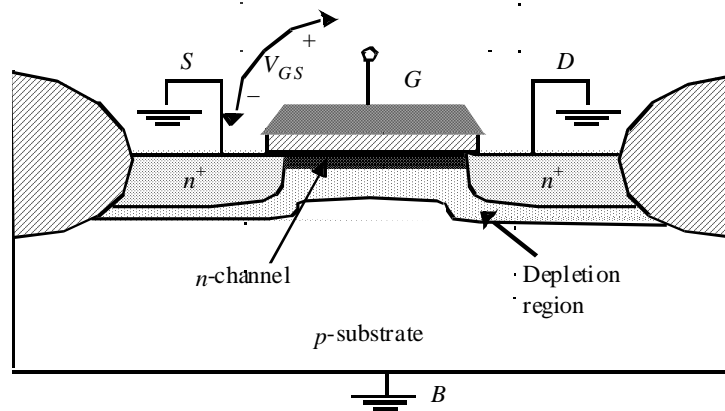
PMOS Enhancement



NMOS with
Bulk Contact

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Threshold Voltage: Concept



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The Threshold Voltage

Threshold
$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|})$$

Fermi potential
$$\phi_F = \phi_T \ln\left(\frac{N_A}{n_i}\right)$$

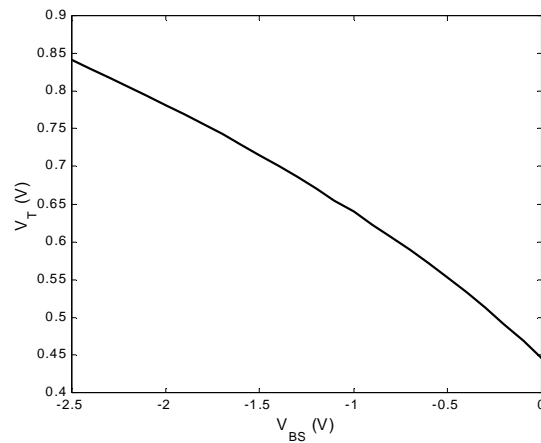
$2\phi_F$ is approximately -0.6V for p-type substrates

γ - the body factor

V_{T0} is approximately 0.45V for our process

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The Body Effect



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The Drain Current

Charge in the channel is controlled by the gate voltage:

$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T] \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Drain current is proportional to charge and velocity:

$$I_D = -v_n(x)Q_i(x)W$$

$$v_n = -\mu_n \xi(x) = \mu_n \frac{dV}{dx}$$

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The Drain Current

Combining velocity and charge:

$$I_D dx = \mu_n C_{ox} W (V_{GS} - V - V_T) dV$$

Integrating over the channel:

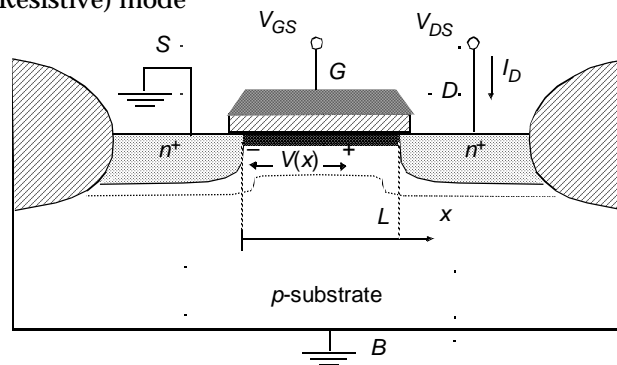
$$I_D = k_n \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] = k_n \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Transconductance: $k_n' = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$

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Transistor in Linear

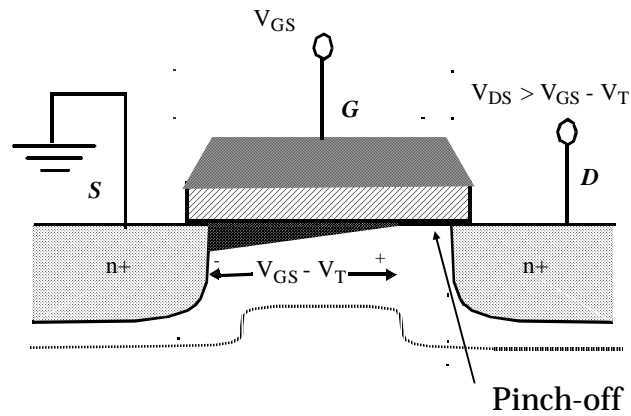
Linear (Resistive) mode



MOS transistor and its bias conditions

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Transistor in Saturation



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Saturation

For $V_{GD} < V_T$, the drain current saturates

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2$$

Including channel-length modulation

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

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Modes of Operation

Cutoff:

$$V_{GS} < V_T$$

$$I_D = 0$$

Resistive:

$$V_T < V_{GS}; V_{GS} - V_T > V_{DS}$$

$$I_D = \frac{k'_n W}{2 L} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right]$$

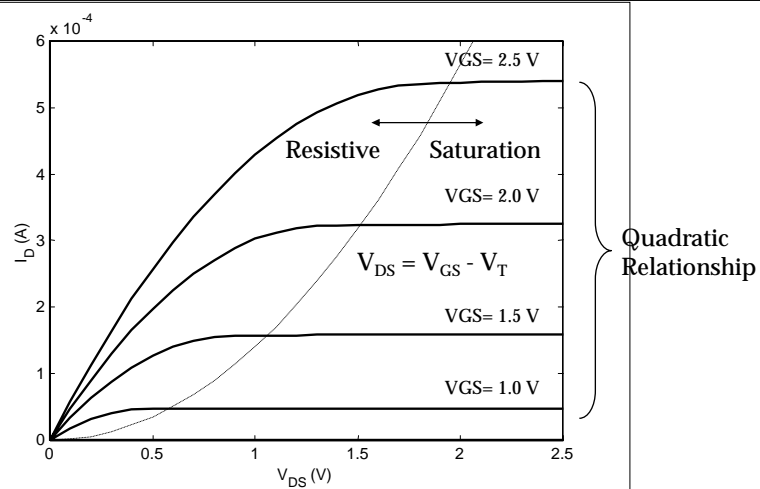
Saturation:

$$V_T < V_{GS}; V_{GS} - V_T < V_{DS}$$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2$$

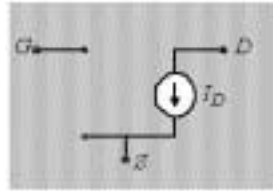
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Current-Voltage Relations A Good Ol' Transistor



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A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$V_{DS} < V_{GS} - V_T$$

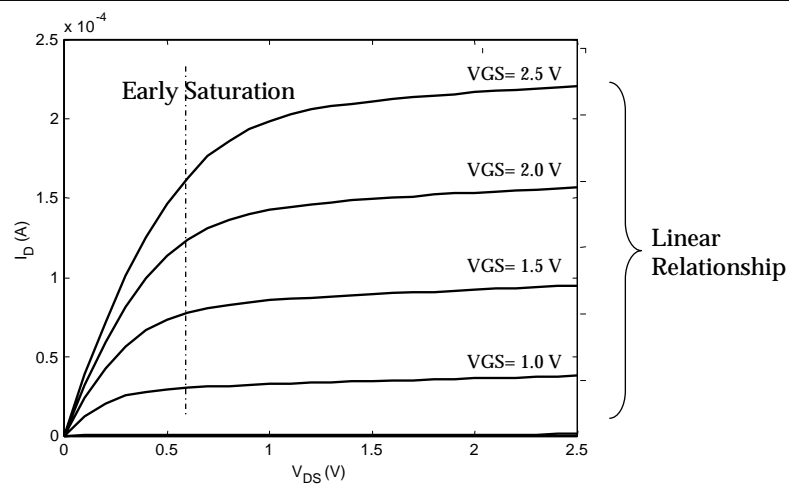
$$I_D = k_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$V_T = V_{T0} + \gamma \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|} \right)$$

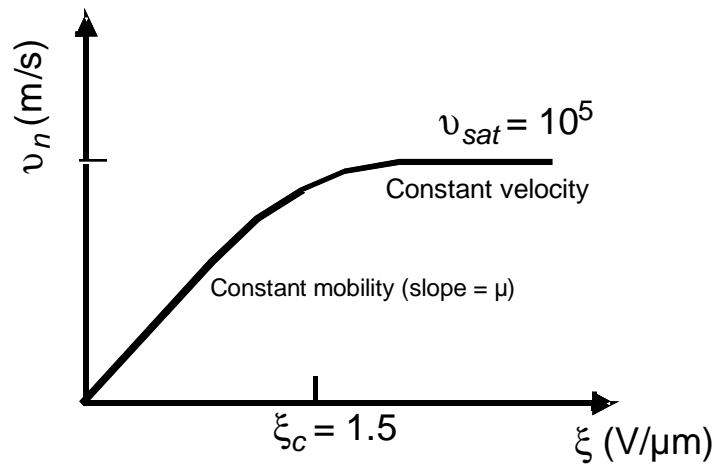
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Current-Voltage Relations The Deep-Submicron Era



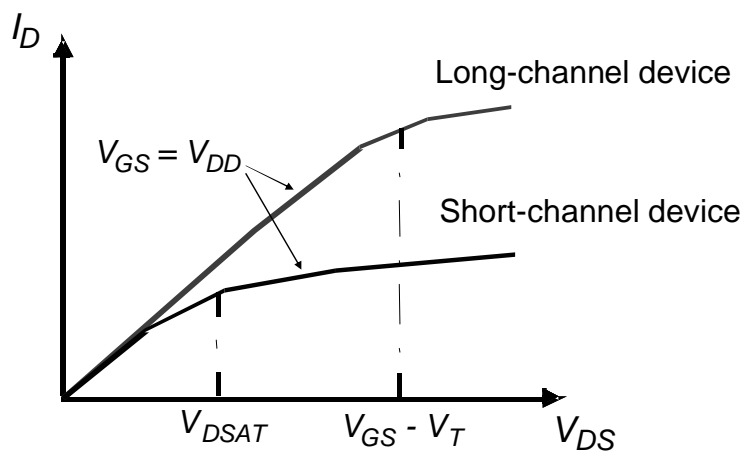
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Velocity Saturation



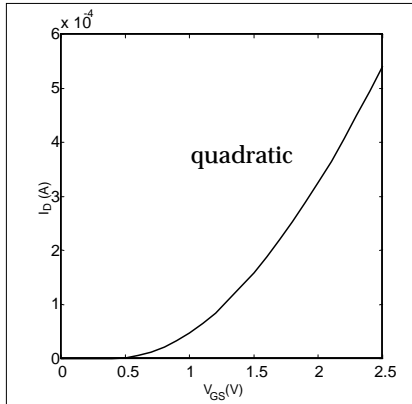
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Velocity Saturation

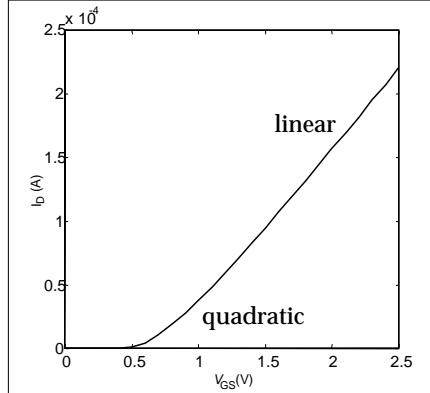


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I_D versus V_{GS}



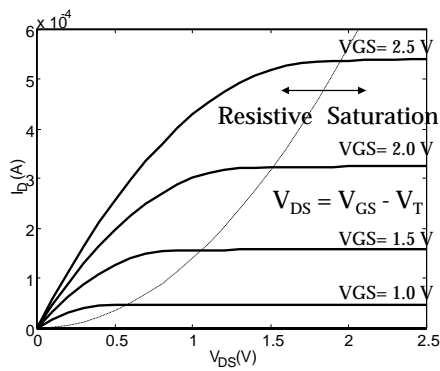
Long Channel



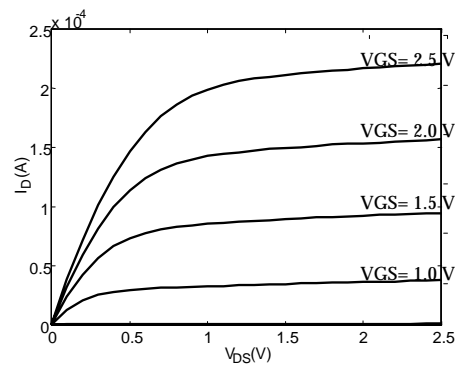
Short Channel

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I_D versus V_{DS}



Long Channel



Short Channel

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Including Velocity Saturation

Approximate velocity:

$$v = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for } \xi \leq \xi_c$$

$$= v_{sat} \quad \text{for } \xi \geq \xi_c$$

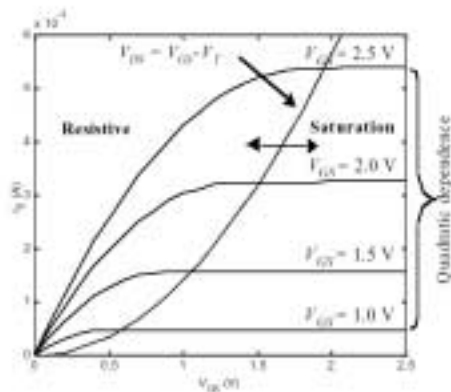
And integrate current again:

$$I_D = \frac{\mu_n C_{ox}}{1 + (V_{DS}/\xi_c L)} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

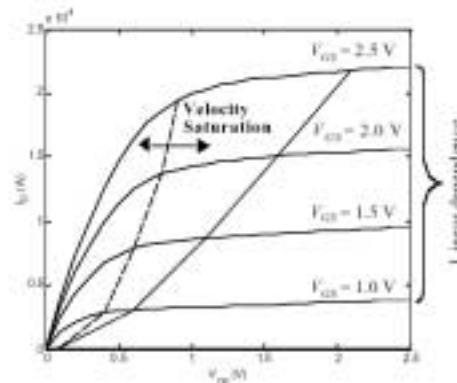
In deep submicron, there are four regions of operation:
 (1) cutoff, (2) resistive, (3) saturation and (4) velocity saturation

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Regions of Operation



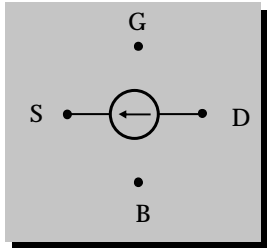
Long Channel



Short Channel

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An Unified Model for Manual Analysis



$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L} \left(V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

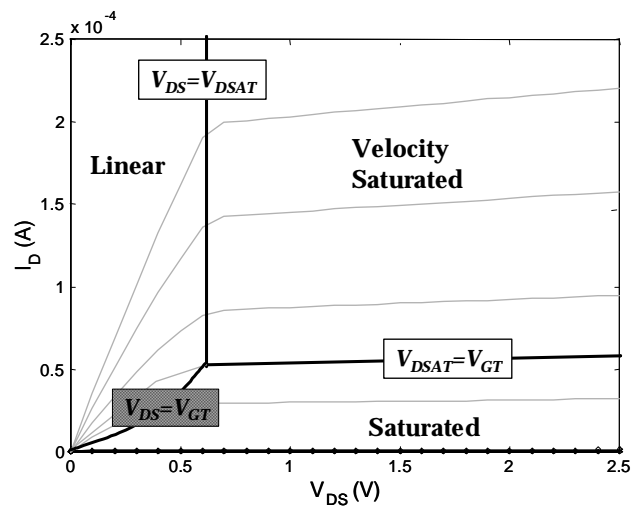
$$\text{with } V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}),$$

$$V_{GT} = V_{GS} - V_T,$$

$$\text{and } V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

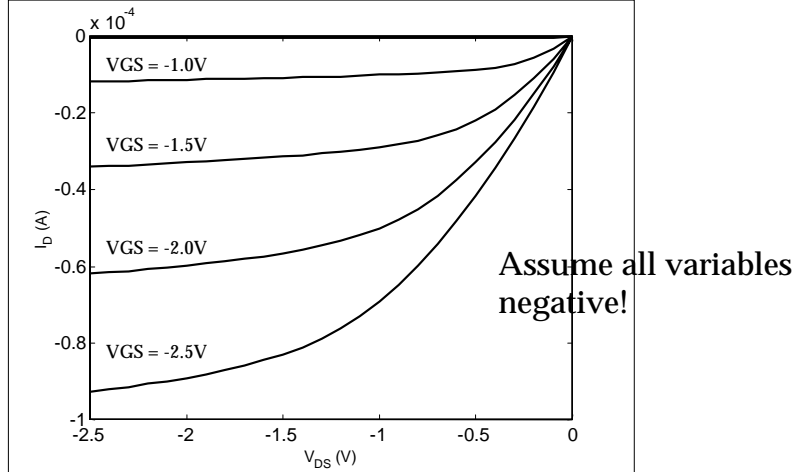
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Regions of Operation



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A PMOS Transistor



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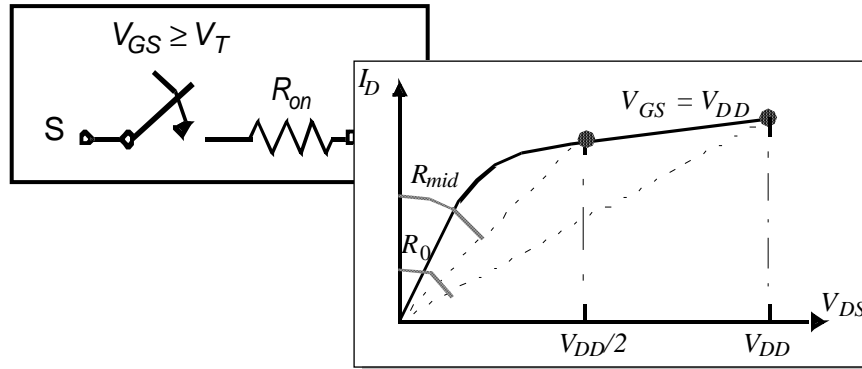
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($\text{V}^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

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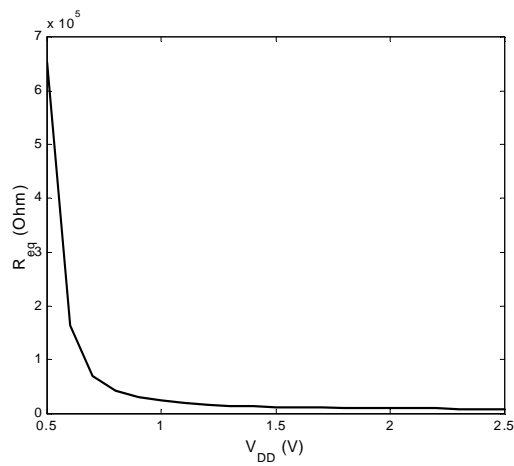
The Transistor as a Switch



$$R_{eq} = \frac{1}{2} \left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD} \right)$$

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The Transistor as a Switch



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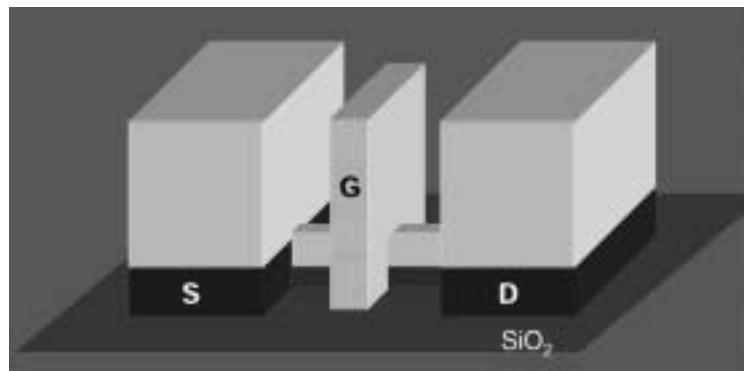
The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} ($W/L = 1$) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L .

V_{DD} (V)	1	1.5	2	2.5
NMOS (k Ω)	35	19	15	13
PMOS (k Ω)	115	55	38	31

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Future Perspectives



25 nm MOS transistor (Folded Channel)

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