Variable-Taper CMOS Buffer

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Abstract—**A variable-taper (VT) approach to buffer design is proposed where the taper from one inverter stage to the next is a function of the position of the inverter within the buffer chain. Though the minimum delay obtained by using a VT buffer is about 15% more than the minimum delay obtained from conventional fixed-taper (FT) buffers, a small modification to the initial stages of the VT buffer reduces this difference to less than 2%. For similar delays, a VT buffer usually takes less area and consumes less power than an FT buffer.**

I. Introduction

With the scaling down of device dimensions, the difference in capacitance of the logic circuitry and the output stages is ever increasing. Lin and Linholm [1] used a tapered chain of inverters where each inverter in the buffer chain drives another inverter which is β_f times its own size. Several authors improved this model to include the no-load delays of the logic gate [2], short-circuit currents in the signal transients [3], and the effect of the output capacitance of the driving stage [4]–[9]. We propose a tapered buffer model of which the taper factor from one inverter stage to the next is a variable dependent on the location of the inverter in the buffer chain. Two important factors considered in the design of the buffers are the delay penalty factor D and the area penalty factor A. The delay penalty factor is the ratio of the propagation delay of the buffer chain to the propagation delay of a logic-level inverter. The area penalty factor is the ratio of the buffer area to the area of a logic-level inverter. In Section II, A and D are derived for a variable-taper (VT) buffer. In Section III, the results are extended to include the self-load capacitance of the driving inverter in the VT buffer design. Comparisons of power dissipations of fixed-taper (FT) and VT buffers are made in Section IV. A modification to VT buffer design that reduces the delay penalty factor of the buffer is presented in Section V.

II. Variable-Taper (VT) Buffer

The taper configuration of the n-stage VT buffer is shown in Fig. 1. The buffer is connected between logic circuitry and output capacitance. The capacitance of the logic-level inverter is given as C_i, the logic-level conductance is g_i, and the logic-level inverter has a first-order RC delay estimate of τ ($\tau = C_i/g_i$) [6]. The sizes of the transistors in stages $k+1$ and k are related by

$$\left(\frac{W}{L}\right)_{k+1} = \beta_v^{k+1}\left(\frac{W}{L}\right)_k \tag{1}$$

where β_v is a taper factor. Therefore, the sizes of the inverters in later stages of the buffer taper out at a greater rate compared to the initial stages. The conductance, load, and delay of the kth stage are

$$g_k = \beta_v^{k(k+1)/2} g_i \tag{2}$$

$$C_k = \beta_v^{(k+1)(k+2)/2} C_i \tag{3}$$

$$\tau_k = \beta_v^{k+1}\tau. \tag{4}$$

The overall delay of the buffer, τ_{ov}, is given as

$$\tau_{ov} = \sum_{k=0}^{n-1} \tau_k = \tau\left(\beta_v + \beta_v^2 + \beta_v^3 + \cdots + \beta_v^n\right) = \frac{\beta_v^n - 1}{\beta_v - 1}\beta_v\tau. \tag{5}$$

To drive a capacitive load of C_L, the number of stages in the buffer, n, is given by

$$n = \frac{1}{2}\left(\sqrt{\frac{8\ln(C_L/C_i)}{\ln(\beta_v)} + 1} - 1\right). \tag{6}$$

The delay penalty factor for the VT buffer, D_v, is given as

$$D_v = \frac{\tau_{ov}}{\tau} = \frac{\beta_v(\beta_v^n - 1)}{\beta_v - 1}. \tag{7}$$

The area penalty factor for the variable taper buffer, A_v, is given by

$$A_v = \sum_{k=0}^{n-1} \beta_v^{k(k+1)/2}. \tag{8}$$

The expression for optimum β_v value for minimum delay in the buffer is given in [10] and Table I gives the optimal β_v for the VT buffer for different ratios of C_L/C_i. It can be seen that $\beta_{v\,\mathrm{opt}}$ reduces for increasing values of the C_L/C_i. This is in contrast to the FT model where the optimal delay is obtained when $\beta_f = e$ for all C_L/C_i ratios [11].

The area penalty factor and delay penalty factor are plotted for different ratios of C_L/C_i for FT and VT

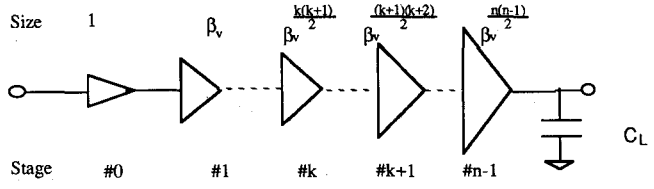

Fig. 1. VT model of a buffer.

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TABLE I
BETA VALUE FOR A MINIMUM DELAY OF A VT BUFFER AND COMPARISON OF THE MINIMUM DELAYS OF FT AND VT BUFFER DESIGNS FOR DIFFERENT CAPACITIVE LOADS

C_L/C_I	10	30	100	300	1000	3000	10000
$\beta_{v\,\mathrm{opt}}$	1.72	1.45	1.37	1.22	1.19	1.17	1.15
$D_{v,\mathrm{opt}}$	6.66	10.04	13.75	17.14	20.85	24.24	27.96
$D_{f,\mathrm{opt}}$	6.26	9.25	12.52	15.50	18.78	21.76	25.04

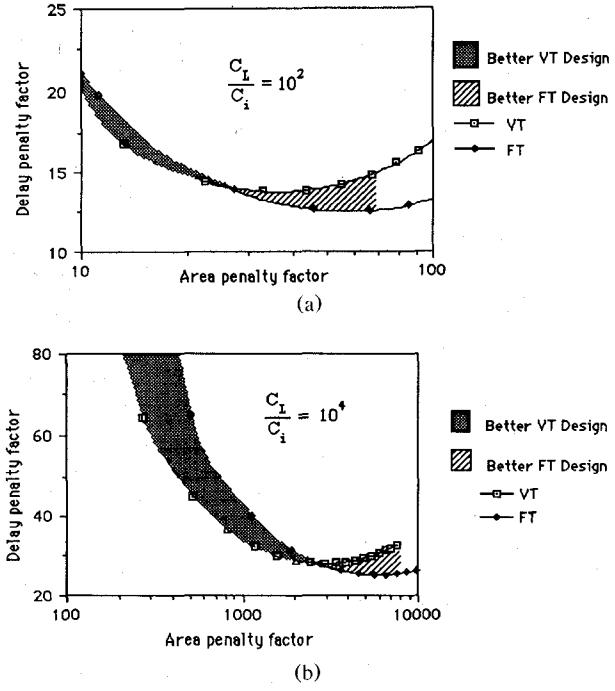

Fig. 2. Comparison of the delay penalty factor versus the area penalty factor of an FT buffer and a VT buffer design for different capacitive loads: (a) $C_L/C_i = 10^2$ and (b) $C_L/C_i = 10^4$.

buffer implementations in Fig. 2(a) and (b). Each point on these curves corresponds to a beta value. The beta values corresponding to the left of the minimum delay factor give good designs; i.e., as the area penalty increases, the delay penalty decreases. For the beta values corresponding to the points on the curve to the right of the minimum delay penalty factor, the area penalty factor increases with increasing delay penalty factor. The shaded region corresponds to the region where the VT model gives a better design, i.e., for the same delay, the area taken by the VT buffer is less than that of the FT buffer, whereas the FT model gives better designs in the cross-hatched areas. In medium fan-out circuits ($C_L < 50C_i$) that require a one- or two-staged buffer, an FT model results in better designs. But, for driving high capacitive loads like off-chip circuitry, control drivers, and clock drivers, a VT buffer results in more compact layouts for comparable delay penalties. The minimum delay in a buffer chain is obtained when the taper from one inverter stage to the next is constant [12], i.e., the FT designs give the minimum possible delays. Table I gives the minimum delays obtained by using FT and VT implementations. The smallest delays obtained using the VT model are less than 15% greater than the smallest delays obtained from an FT model.

III. Effect of the Output Capacitance on the Buffer Design

The effect of the inherent output capacitance in the design of an FT buffer was discussed by Li *et al.* [6]. The approach used is to split the output capacitance into two parts: an inherent output capacitance C_x of the driver stage and a load capacitance C_y of the driven stage. The logic-level value of the capacitance is $C_x + C_y$. The logic-level delay is given as

$$\tau_i = \frac{C_x + C_y}{g} = \left(\frac{C_x}{C_y} + 1\right)\tau = \frac{\tau}{p} \tag{9}$$

where

$$p = \frac{C_y}{C_x + C_y}. \tag{10}$$

The optimum β_f for minimum delay for an FT buffer [6] can be obtained from

$$\beta_f\left[\ln(\beta_f) - 1\right] = \frac{C_x}{C_y}. \tag{11}$$

For a VT buffer, the delay of the kth stage is given as

$$\tau_k = \frac{\beta_v^{k(k+1)/2} C_x + \beta_v^{(k+1)(k+2)/2} C_y}{\beta_v^{k(k+1)/2} g} = \left[1 + \left(\beta_v^{k+1} - 1\right)p\right]\tau_i. \tag{12}$$

The delay of the buffer is given as

$$\tau_{ov} = \sum_{k=0}^{n-1} \left(1 + \left(\beta_v^{k+1} - 1\right)p\right)\tau_i = \left[n(1-p) + \frac{\beta_v(\beta_v^n - 1)}{\beta_v - 1}p\right]\tau_i. \tag{13}$$

The expression for the β_v that results in minimum propagation delay is given in [13] and Table II gives the optimal beta values for different capacitive loads and also for different ratios of C_x/C_y. The β_v for minimum delay depends on both C_L/C_y and C_x/C_y ratios.

IV. Power Dissipation Considerations of a CMOS Buffer

Power dissipation in an inverter during input signal transition consists of two parts:

$$\text{dynamic dissipation: } P_1 = C_{\mathrm{load}} V^2 f \tag{14}$$

$$\text{short-circuit dissipation: } P_2 = I_{\mathrm{mean}} V. \tag{15}$$

Most of the power is dissipated in the later stages of the buffer because of the large load capacitances that contribute to the larger dynamic power dissipation and wider transistors that contribute to a larger short-circuit power dissipation. For a given capacitive load C_{load} and switching frequency f, the dynamic power dissipation is almost constant. The dynamic power dissipation is proportional to the load capacitance, which is a function of

TABLE II
OPTIMAL BETA ($\beta_{v\,opt}$) VALUES OF SPLIT-CAPACITOR VT BUFFER MODEL FOR DIFFERENT VALUES OF C_L/C_y AND C_x/C_y

$\frac{C_x/C_y}{C_L/C_y}$	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.8	1.0	2.0	5.0
10	1.723	1.788	1.849	1.916	1.978	2.038	2.107	2.229	2.362	3.031	5.359
10^2	1.316	1.340	1.364	1.387	1.412	1.435	1.457	1.500	1.541	1.741	2.281
10^3	1.201	1.216	1.231	1.245	1.259	1.272	1.285	1.311	1.336	1.449	1.731
10^4	1.148	1.158	1.169	1.179	1.188	1.198	1.207	1.225	1.242	1.320	1.509

TABLE III
COMPARISON OF AREAS AND POWER DISSIPATIONS OF VT AND FT BUFFER DESIGNS WITH SIMILAR PROPAGATION DELAYS

$\frac{C_L}{C_i}$ ratio	Buffer type and number of stages	Area penalty factor	Delay (ns)	Average power (mW)	Dynamic power (mW)	Short circuit (sc) power	% of sc power in total power
100	FT 2	11	9.25	0.568	0.536	0.0318	5.68
100	VT 2	5.64	9.57	0.503	0.481	0.0125	2.48
100	VT 3	13	9.18	0.580	0.549	0.031	5.31
1000	FT 3	111	11.92	5.74	11.18	0.3005	2.62
1000	VT 4	74	11.32	5.26	8.828	0.1524	1.70
1000	FT 4	216	10.61	6.73	5.878	0.852	12.66
1000	VT 6	178	11.0	6.32	5.677	0.643	10.17
10000	FT 3	486	18.73	51.56	48.47	3.03	5.88
10000	VT 4	271	16.42	48.03	46.09	1.945	4.05
10000	FT 4	1111	14.03	57.52	54.65	2.851	4.96
10000	VT 6	820	13.42	53.84	51.96	1.84	3.41
10000	FT 5	1883	13.05	65.14	60.95	4.192	6.44
10000	VT 8	1575	13.07	61.23	57.66	3.571	5.83

the total area of the buffer. In general, for similar delay penalties, an FT buffer takes more area than a VT buffer and hence more dynamic power dissipation.

The short-circuit power dissipation is a function of both the output load capacitance as well as the input transition time. A good index that takes care of both the input transition time and output capacitive load is the output transition time. Short-circuit power dissipation is directly proportional to the ratio of input transition time to output transition time [3]. When the input transition time is comparable to output transition time, then the short-circuit power dissipation is less than 20% of the dynamic power dissipation [3]. As the input transition time becomes less than the output transition time, the percentage of short-circuit power dissipation in the total power dissipation reduces further [3]. In FT buffers, the input transition times at all the stages are almost equal to output transition times because of similar relative loading (ratio of capacitive load to the size of the driving transistors) from one stage to the next. This assumption is valid if ratios of PMOS and NMOS transistors are used that result in symmetrical rise and fall times. In VT buffers, the input transition time at any stage is always less than its output transition time. Thus, the ratio of short-circuit power dissipation to dynamic power dissipation of a VT buffer is less than that of an FT buffer. Since, the dynamic power dissipation of a VT is less than that of an FT, the short-circuit power dissipation will be still less. Hence, the power dissipation in a VT buffer is less than that of an FT buffer.

To verify the qualitative discussion above, we ran SPICE simulations on some VT and FT buffer implementations that have similar propagation delays. The power dissipation was measured using the power meters proposed by Kang [14]. The short-circuit power dissipation is obtained by using the method developed by Yacoub and Ku [15]. In Table III, the buffer areas and power dissipations of some FT and VT buffer designs with similar propagation delays and capacitive loads are compared. From the comparisons we can see that the VT approach gives better designs, i.e., less power dissipation and less area compared to FT buffer designs for higher ratios of C_L/C_i. But for a C_L/C_i ratio of 100 there is not much difference between the VT or FT buffer designs. For still lower ratios of C_L/C_i, the FT approach gives better results. In general, dynamic power dissipation is higher in designs that take more area, usually FT buffer designs. Also, the percentage of short-circuit power dissipation in the total power dissipation in VT buffers is less than the values seen in FT buffers, as shown in column 8 of Table III.

V. REDUCING THE DELAY PENALTY OF A VT BUFFER

From Tables I and II, it can be observed that the optimal values of beta, $\beta_{v\,opt}$, for a VT buffer range from 1.15 to 5.36. Also, $\beta_{v\,opt}$ reduces with increasing ratios of C_L/C_y, resulting in a larger number of inverter stages. Because of the low values of β_v, the taper in the first few stages of a VT buffer is very small. Therefore, the initial

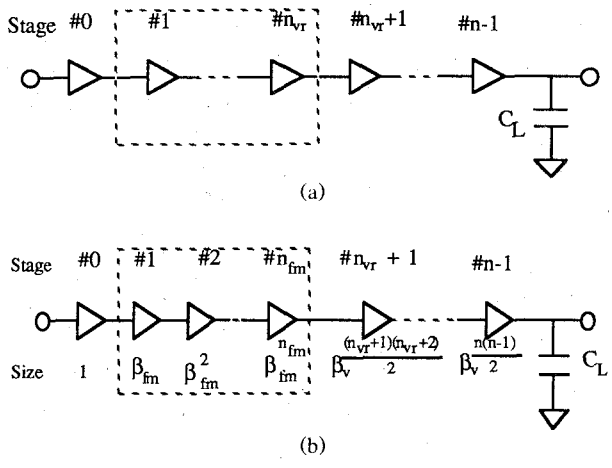

Fig. 3. (a) A VT buffer with the first n_{vr} stages to be replaced. (b) Modified VT buffer using n_{fm} modified fixed-taper stages.

inverter stages take more area and also increase the delay. These stages contribute significantly to the difference in the minimum delay penalty factors of FT and VT buffers. To improve the buffer performance, the first n_{vr} stages of a VT buffer are replaced with n_{fm} stages having a fixed-taper β_{fm} as shown in Fig. 3(a) and (b), where

$$n_{vr} = \frac{1}{2}\sqrt{\frac{8n_{fm}}{\ln \beta_v}\left(1+\frac{C_x}{eC_y}\right)} - 1 \tag{16}$$

and the fixed-taper factor for the replacing n_{fm} modules, β_{fm}, is given by

$$\beta_{fm} = \beta_v^{n_{vr}(n_{vr}+1)/(2n_{fm})}. \tag{17}$$

The delay penalty factor D_m and the area penalty factor A_m are given as

$$D_m = (1-p)(n+n_{fm}-n_{vr}) + pn_{fm}\beta_{fm} + p\frac{\beta_v^{n+1} - \beta_v^{n_{vr}+1}}{\beta_v - 1} \tag{18}$$

and

$$A_m = \frac{\beta_{fm}^{n_{fm}} - 1}{\beta_{fm} - 1} + \sum_{k=n_{fr}+1}^{n-1} \beta_v^{k(k+1)/2}. \tag{19}$$

The delay penalties obtained from implementation of a buffer using an FT buffer, a VT buffer, and modified VT buffers with n_{fm} varying from 1 to 4 are plotted against area penalty factor in Fig. 4. The modified VT buffer gives better results than a VT buffer in the entire $A-D$ domain. The minimal delay penalty obtained with a four-n_{fm}-stage modified VT buffer is within 2% of the minimal delay penalty of an FT implementation compared to nearly 12% for the VT buffer with a C_L/C_i ratio of 1000. Also, the minimal delay of the modified VT approaches the minimal delay of an FT with increasing number of modified stages (n_{fm}). Compared to an FT buffer, the modified VT gives the best results over almost the entire $D-A$ region except when absolute minimum delays are required. The modified VT buffer also results in almost the same minimum delays as an FT buffer when the output capacitance of the driving stage is included as shown in Fig. 5, where the C_x/C_y ratio is 0.4.

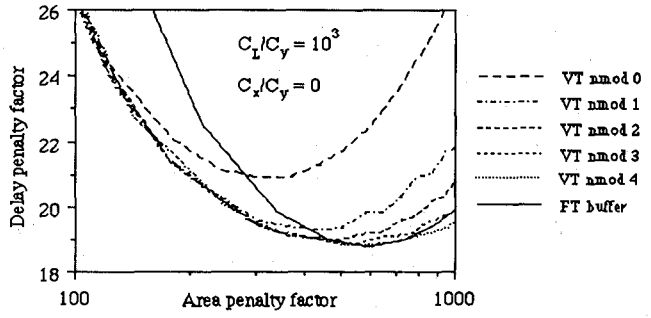

Fig. 4. Comparison of the delay penalty factors of an FT buffer, a VT buffer, and modified VT buffers with n_{fm} 1 to 4 for a C_L/C_i ratio of 10^3.

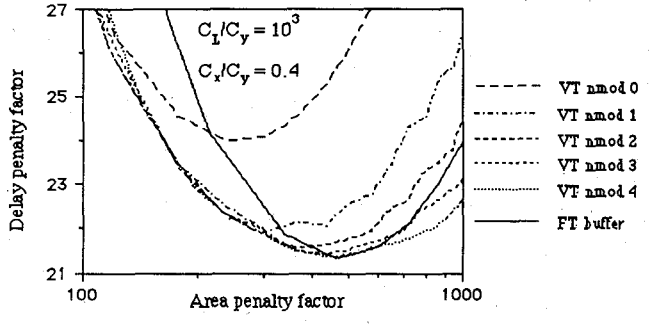

Fig. 5. Comparison of the delay penalty factors of an FT buffer, a VT buffer, and modified VT buffers with n_{fm} 1 to 4 using split-capacitive loads. $C_L/C_y = 10^3$; $C_x/C_y = 0.4$.

VI. Conclusions

A new approach using a variable taper (VT) in the design of buffer stages is proposed. This results in very significant area savings but the minimum delay is longer than that of traditional FT model. For similar propagation delays, the power dissipation of a VT buffer is also less than an FT design. A modification to the VT gives almost the same minimal delay as the FT, with significant area savings. The results indicate that the modified VT gives better designs for high capacitive loads ($50C_i$–$10000C_i$) whereas the FT is optimal in applications with medium capacitive loads ($5C_i$–$50C_i$).

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References

[1] H. C. Lin and L. W. Linholm, "An optimized output stage for MOS integrated circuits," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 2, pp. 106–109, Apr. 1975.

[2] M. Nemes, "Driving large capacitances in MOS LSI systems,"

IEEE J. Solid-State Circuits, vol. SC-19, no. 1, pp. 159–161, Feb. 1984.

[3] H. J. M. Veendrick, "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 4, pp. 468–473, Aug. 1984.

[4] N. Hedenstierna and K. Jeppson, "CMOS circuit speed and buffer optimization," *IEEE Trans. Computer-Aided Design*, vol. CAD-6, no. 2, pp. 270–281, Mar. 1987.

[5] V. N. R Rayapati and S. Mahapatra, "Very large scale integrated CMOS buffer design," *Microelectron. Rel.*, vol. 29, no. 6, pp. 1021–1033, 1989.

[6] N. C. Li, G. L. Haviland, and A. A. Tuszynski, "CMOS tapered buffer," *IEEE J. Solid-State Circuits*, vol. 25, no. 4, pp. 1005–1008, Aug. 1990.

[7] A. J. Al-Khalili, Y. Zhu, and D. Al-Khalili, "A module generator for optimized CMOS buffers," *IEEE Trans. Computer-Aided Design*, vol. 9, no. 10, pp. 1028–1046, Oct. 1990.

[8] M. Annaratone, *Digital CMOS Circuit Design*. Norwell, MA: Kluwer Academic, 1986, pp. 155–163.

[9] L. A. Glasser and D. W. Dobberpuhl, *The Design and Analysis of VLSI Circuits*. Reading, MA: Addison-Wesley, 1985, pp. 253–265.

[10] S. R. Vemuru and E. D. Smith, "Variable taper CMOS buffer design," in *Proc. 9th Biennial Univ. Govt. Ind. Microelectron. Symp.*, 1991, pp. 179–184.

[11] R. C. Jaeger, "Comments on 'An optimized output stage for MOS integrated circuits'," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 3, pp. 185–186, June 1975.

[12] M. Shoji, *CMOS Digital Circuit Technology*. Englewood Cliffs, NJ: Prentice-Hall, 1987, pp. 366–369.

[13] S. R. Vemuru and E. D. Smith, "Split-capacitive load variable taper buffer design," in *Proc. 34th Midwest Symp. Circuits Syst.*, 1991, pp. 923–926.

[14] S. M. Kang, "Accurate simulation of power dissipation in VLSI circuits," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 889–891, no. 5, Oct. 1986.

[15] G. Y. Yacoub and W. H. Ku, "An enhanced technique for simulating short-circuit power dissipation," *IEEE J. Solid-State Circuits*, vol. 24, no. 3, pp. 844–847, June 1989.