Problem 1 – Extracting Unified Model Parameters from Simulation
The objective of this problem is to simulate a complex transistor model using SPICE, extract fundamental information from the results to build an approximate transistor model for use in hand calculations, and then compare the two models.

1A Using SPICE, generate the family of I-V curves for an NMOS transistor with the following parameters:

W/L = 10u/.5u
Sweep VDS from 0V to 2.0V in 0.1V increments
VGS = 0.4V, 0.8V, 1.2V, 1.6V, 2.0V
VSB = 0V, 1.0V

For this problem use a generic 0.5um model by adding the following line to your SPICE deck or copying the same file to your own account or workstation:

.lib '/home/ff/ee141/MODELS/g25.mod' TT

Soln: The following Spice deck is written to generate the family of curves:

* EE141 SPRING 2005 HW2 PROB 1A
* Generates family of I-V curves for a given NMOS model
* Reference transistor model
.lib '/home/ff/ee141/MODELS/g25.mod' TT

* parameters
.param sb = 0

* Netlist to probe the transistor
M1 drain gate source bulk NMOS w=10u l=0.5u

* three DC voltage sources to apply test signals
VDS drain 0 0
VGS gate source 0
VSB source bulk sb

* connect the source to ground with a 0 V source
VSOURCE source 0 0

* format output for use in AWaves
.options post=2

* DC sweep with VDS as the inner sweep, and outer loops
* set different values for VGS and VSB. Recall
* that the source terminal is fixed at 0 potential.
The Spice deck is simulated with HSpice, and the resulting plot is generated in AWaves:

IB Based on the results from the previous part, determine the following model parameters: $V_{T0}$, $k_p$, $\lambda$, $\gamma$. You may assume that velocity saturation doesn’t play a significant role and $-2\Phi_F = 0.6$V.

Soln: There are multiple ways to extract these parameters, but a simple method is as follows.
VT0: Select two points in the saturation region from different VGS curves, but with VSB=0 and the same VDS in both cases. This allows us to extract VT0 from the unified model equations. The points can be measured directly in AWaves or graphically from the result in 1A.

<table>
<thead>
<tr>
<th>Point</th>
<th>VGS (V)</th>
<th>VDS (V)</th>
<th>ID (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.8</td>
<td>1.5</td>
<td>200</td>
</tr>
<tr>
<td>B</td>
<td>1.2</td>
<td>1.5</td>
<td>1.08</td>
</tr>
</tbody>
</table>

VT0=0.49V

\[ \lambda \text{ is extracted with the same method, this time picking two points with the same VGS but differing VDS:} \]

<table>
<thead>
<tr>
<th>Point</th>
<th>VGS (V)</th>
<th>VDS (V)</th>
<th>ID (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.6</td>
<td>1.4</td>
<td>2.04</td>
</tr>
<tr>
<td>B</td>
<td>1.6</td>
<td>2.0</td>
<td>2.08</td>
</tr>
</tbody>
</table>

\[ \lambda = 0.036 \]

\( \gamma \) is extracted the same way with VDS and VGS held constant and varying VSB

<table>
<thead>
<tr>
<th>Point</th>
<th>VSB (V)</th>
<th>VGS (V)</th>
<th>VDS (V)</th>
<th>ID (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>1.6</td>
<td>2.0</td>
<td>1.54</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>1.6</td>
<td>2.0</td>
<td>2.08</td>
</tr>
</tbody>
</table>

\[ \gamma \text{ is extracted the same way with VDS and VGS held constant and varying VSB} \]
\[ V_T = 0.65V \]

Now, use the body effect formula:

\[ V_T - V_{T_0} = \gamma \left( \sqrt{V_{SB}} - 2\Phi_F \right) - \sqrt{2\Phi_F} \]

\[ \gamma = 0.33V^{1/2} \]

\[ kp \] is found by plugging a single point into the saturation current equation:

Point VSB VGS VDS ID
A 0V 2V 2.0V 3.2mA

\[ 3.2mA = 0.5*20*kp(2-0.49)^2(1+0.036*2) \]

\[ kp = 133\mu A/V^2 \]

1C Starting with the SPICE deck used in the first part, add your own simple transistor model using the parameters determined above. This should be of the form

```plaintext
.model nmos_simple NMOS (LEVEL = 1 + VT0=?? KP=?? GAMMA=?? LAMBDA=?? PHI=0.6)
```

Generate the family of I-V curves for an NMOS transistor with the following parameters, showing simulation of both the original model and your own simplified model on the same plot. Comment on any differences.

Soln: The new spice deck is as follows:

```plaintext
* EE141 SPRING 2005 HW2 PROB 1C
* Generates family of I-V curves for a given NMOS model
* and a simpler approximate model
* Reference transistor model
.lib `/home/ff/ee141/MODELS/g25.mod` TT
* approximate model

.model nmos_simple NMOS (LEVEL = 1 + VT0=0.49 KP=133e-6 GAMMA=0.33 LAMBDA=0.036 PHI=0.6)
* paramters
.param sb = 0

* Netlist to probe the two transistors
M1 drain gate source bulk NMOS w=10u l=.5u
```
M2 drain gate source2 bulk nmos_simple w=10u l=.5u

* three DC voltage sources to apply test signals
VDS drain 0 0
VGS gate source 0
VSB source bulk sb

* connect the sources to ground with 0 V supplies
* this fixes the absolute voltage levels in the circuit wrt ground
* and also provides a way to measure the drain current, because
* hspice will save the currents through these supplies
VSOURCE source 0 0
VSOURCE2 source2 0 0

* format output for use in AWaves
.options post=2

* DC sweep with VDS as the inner sweep, and outer loops
* set different values for VGS and VSB. Recall
* that the source terminal is fixed at 0 potential.
.DC VDS 0 2 0.1 VGS 0.4 2 0.4
.plot DC I(M1) I(M2)
.end

AWaves is used to plot the resulting two families on a single plot shown above.
There are two main differences:
1) In the saturation region the level 1 model predicts too much current for high VGS, too little current for low VGS

2) In most cases the current in the linear region is too low in the simple model, even for gate voltages where the saturation current is close to the original model. Another way of looking at this is that in the linear region the level 1 model generally predicts a weaker device, but the linear region extends to higher values of VDS.

These differences are consistent with the fact that short channel effects are neglected in the level 1 model, but not the original model. Compared with the quadratic level 1 model, we see that $I_d$ grows slower than quadratic with $V_{GS}-V_T$ in the full model, and saturation is reached at lower values of $V_{DS}$ for a given $V_{GS}$.

The slope of the curves in the saturation region is similar in both models.
Problem 2 – Generating a Voltage Transfer Characteristic

2A Draw the VTC for this circuit. Determine (or estimate, if necessary, from your VTC) the following parameters: $V_{OH}$, $V_{OL}$, $V_M$

We are given both load line plots for the active NMOS device and the non-linear device of the shaded box. How do we link the information provided by these curves to generate information about input and output voltages? First, we need to realize that the output voltage of the NMOS device determines what the voltage drop across the shaded box. That is,

$$V_{out} = V_{DS} = V_{DD} - V_{shaded-box}$$

Since we know I-V relationships in each device AND also the fact that the current through one must be equal to the current through the other, we can manipulate the curves to tell us something. Using the relation above, we can superimpose a horizontally-flipped version of the shaded-box’s I-V curve onto that of the NMOS’ curves. The intersections are the operating points of this circuit and will give us the input-output voltage relationships we need to build our VTC. Below is the revised, superimposed graph with the intersections labeled:
<table>
<thead>
<tr>
<th>Point</th>
<th>Vin (VGS)</th>
<th>Vout (VDS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2.4V</td>
<td>0.57V</td>
</tr>
<tr>
<td>B</td>
<td>2.0V</td>
<td>0.7V</td>
</tr>
<tr>
<td>C</td>
<td>1.6V</td>
<td>0.97V</td>
</tr>
<tr>
<td>D</td>
<td>1.2V</td>
<td>1.4V</td>
</tr>
<tr>
<td>E</td>
<td>0.8V</td>
<td>2.2V</td>
</tr>
<tr>
<td>F</td>
<td>0.4V</td>
<td>2.5V</td>
</tr>
<tr>
<td>G</td>
<td>0.0V</td>
<td>2.5V</td>
</tr>
</tbody>
</table>

The resolution of our plot will not be as fine as we’d like, but you can see how if we had more points, the curve becomes more and more accurate. This VTC is plotted using Matlab. You can also do it by hand.

Looking at the VTC, it is quite easy to determine what VOH, VOL, and VM are:

VOH  **2.5V**  -- NMOS off, shaded-box offers resistive path to bring Vout high, assuming the output is driving a capacitive load or infinite resistance (which is often true for analysis questions like these)
When the NMOS transistor turns on, it tries to pull Vout low. At the same time, the shaded-box is trying to pull Vout high. Depending on the ratio of their effective resistances, $V_{OL}$ will change. This is something that will be discussed later on the semester when Ratioed Logic is covered in the course.

$V_{OL} \approx 0.6V$ – When the NMOS transistor turns on, it tries to pull Vout low. At the same time, the shaded-box is trying to pull Vout high. Depending on the ratio of their effective resistances, $V_{OL}$ will change. This is something that will be discussed later on the semester when Ratioed Logic is covered in the course.

$V_M \approx 1.3V$ – Slightly off the 1.25V we were hoping to get in an ideal symmetrical VTC for an inverter.

This circuit can be used as an alternative to a traditional CMOS inverter (where the non-linear device is a PMOS transistor). From the concepts discussed thus far in lecture and from the results of your VTC, what are the disadvantages of this method?

Incomplete pull-down of the output node means we don’t get full rail-to-rail swing at the output. The noise margin is reduced.

There is static power consumption when the input is high, because there is a direct path from supply to ground when the NMOS transistor is on. Also the high $V_{OL}$ leads to static power consumption in the gate that it drives. For low power applications, we aim to minimize static power.

The VTC also is asymmetric, meaning that a rising transition and its associated output have different large signal and timing characteristics as a falling transition. Uneven noise margin is also another problem.
Problem 3 – VTC and Inverter Analysis

3A

Inverter A

\( V_{OH} \):
First assume that \( V_{OL} < 0.5V \) because we know that the NMOS device is much stronger than the PMOS device for a full VDD input (MUST remember to verify this assumption after finding the solution). In this case we immediately note that \( V_{OH} = V_{DD} = 2.5V \), because when \( V_{IN} = V_{OL} \) the NMOS device is in the cutoff region (\( I_D = 0 \)) and the PMOS device provides a conductive path to VDD.

\( V_{OL} \):
Now, we find \( V_{OL} \) by solving for \( V_{out} \) when \( V_{in} = V_{OH} = 2.5V \). Again, with the assumption that \( V_{OL} < 0.5V \), note that the PMOS device will be in saturation because \( |V_{DS}| > |V_{GS} - V_{TH}| \) and \( |V_{GS}| > |V_{TH}| \). Following the same assumption, the NMOS device is in the triode (linear) region because \( V_{DS} < V_{GS} - V_{TH} \) and \( V_{GS} > V_{TH} \). Thus, the drain currents are given by:

\[
I_{dn} = k_n \frac{W_n}{L_n} \left( V_{GSS} - V_{th} \right) \left( V_{DS} - \frac{V_{DS}^2}{2} \right) = k_n \frac{W_n}{L_n} \left( (V_{DD} - V_{in}) V_{OL} - \frac{V_{OL}^2}{2} \right)
\]

\[
I_{dp} = k_p \frac{W_p}{2} \left( V_{GSP} - V_{th} \right)^2 \left( 1 + \lambda V_{DS} \right) = k_p \frac{W_p}{2} \left( V_{GSP} - V_{th} \right)^2 \left( 1 + \lambda (V_{DD} - V_{OL}) \right)
\]

Solving for \( V_{OL} = 242mV \) (our assumption checks out out)

\( V_{M} \):
To find \( V_{M} \), we follow a similar pattern of assumption followed by verification. Assume that \( V_{M} > 0.5V \); in which case the PMOS device will be operating in the triode region. Since \( V_{IN} = V_{OUT} = V_{M} \) at the midpoint, we see that \( V_{GSS} = V_{DS} \) for the NMOS device, so it is now operating in the saturation region. The drain currents are now given by:

\[
I_{dn} = k_n \frac{W_n}{2} \left( V_{GSS} - V_{th} \right)^2 \left( 1 + \lambda V_{DS} \right) = k_n \frac{W_n}{2} \left( V_{M} - V_{in} \right)^2 \left( 1 + \lambda V_{M} \right)
\]

\[
I_{dp} = k_p \frac{W_p}{2} \left( V_{GSP} - V_{th} \right) V_{DS} - \frac{V_{DS}^2}{2} = k_p \frac{W_p}{2} \left( V_{DD} - V_{in} \right) \left( V_{DD} - V_{M} \right) - \frac{(V_{DD} - V_{M})^2}{2}
\]

Solving numerically, \( V_{M} = 1.27V \)

Inverter B

\( V_{OH} \):
Set $V_{in} = 0$, M1 is off.

$$V_F = V_F^0 + \gamma \left( \sqrt{\frac{-2 \phi_F}{V_{DS}}} + \sqrt{\frac{-2 \phi_F}{V_{DS}}} \right)$$

$$V_{SB} = V_{out}$$

M2 off if:

$$V_{GS} - V_T = V_{DD} - V_{out} - V_T = 0$$

Solve for $V_{out} = \text{V}_{OH} = 1.76 \text{V}$

$\text{VOL}$:

Set $V_{in} = V_{dd} = 2.5 \text{V}$; both M1 and M2 are on and guessing M2 is in saturation because $V_{out}$ will likely be small, while M1 likely in linear region.

$$I_{d1} = k_s \frac{W}{L_n} \left[ (V_{GS} - V_T) \left( \frac{V_{DS}^2}{2} \right) - \left( \frac{V_{DS}^2}{2} \right) \right] = k_s \frac{W}{L_n} \left[ (V_{DD} - V_{out}) \left( \frac{V_{out}^2}{2} \right) - \left( \frac{V_{out}^2}{2} \right) \right]$$

$$I_{d2} = \frac{k_s}{2} \frac{W}{L_n} (V_{GS} - V_T)^2 (1 + \lambda V_{GS}) = \frac{k_s}{2} \frac{W}{L_n} (V_{DD} - V_{out} - V_T) \gamma \left( \sqrt{\frac{-2 \phi_F}{V_{out}}} - \sqrt{\frac{-2 \phi_F}{V_{out}}} \right) (1 + \lambda (V_{DD} - V_{out}))$$

$I_{d1} = I_{d2}$

Solve for $V_{out} = \text{V}_{OL} = 226 \text{mV}$

$\text{VM}$:

Similar to the calculation for $\text{VOL}$ above, except M1 is also in saturation. Equate currents and solve for $V_{out} = \text{V}_{M} = 921 \text{mV}$

Inverter C

$\text{VOH}$:

Since this is a CMOS inverter, $\text{VOH}=2.5 \text{V}$

$\text{VOL}$:

Similarly, $\text{VOL}=0 \text{V}$

$\text{VM}$:

Both devices will be in saturation...

$$I_{d1} = \frac{k_s}{2} \frac{W}{L_n} (V_{GSn} - V_{Tn}) (1 + \lambda V_{GSn}) = \frac{k_s}{2} \frac{W}{L_n} (V_{M} - V_{Tn})^2 (1 + \lambda V_{M})$$

$$I_{d2} = \frac{k_s}{2} \frac{W}{L_p} (V_{GSp} - V_{Tp})^2 (1 + \lambda V_{GSp}) = \frac{k_s}{2} \frac{W}{L_p} (V_{DD} - V_{M} - V_{Tp})^2 (1 + \lambda (V_{DD} - V_{M}))$$

$I_{d1} = I_{d2}$

Solving for $\text{V}_{M}=1.19 \text{V}$
3B
Here’s the HSPICE netlist to verify the results from above:

* EE141 SPRING 2005 HW2 PROB 3

.model nmos NMOS (LEVEL = 1
  + VTO = 0.5 KP = 18e-6 GAMMA = 0.5 LAMBDA = 0.06 PHI = 0.3)

.model pmos PMOS (LEVEL = 1
  + VTO = -0.5 KP = 5e-6 GAMMA = 0.5 LAMBDA = 0.1 PHI = 0.3)

*Inverter A
M1 vout_pn 0 vdd vdd pmos W=1u L=0.5u
M2 vout_pn vin 0 0 nmos W=1.5u L=0.5u

*Inverter B
M3 vdd vdd vout_n 0 nmos W=0.5u L=0.5u
M4 vout_n vin 0 0 nmos W=2.0u L=0.5u

*Inverter C
M5 vout_std vin vdd vdd pmos w=3u l=0.5u
M6 vout_std vin 0 0 nmos w=1u l=0.5u

*Sources
VSUPP vdd 0 2.5
VSRC vin 0 0

.options post=2
.op

.DC VSRC 0 2.5 0.05

.END

This produces the following…
Problem 4 – Propagation Delay and Technology scaling

4A

Inverter A

Pull-down $R_{eq, pd}$:

$R_0$:
\[ I_{ds} = \frac{k_n nW_n}{2 L_n} (V_{OH} - V_T)^2 (1 + \lambda V_{OH}) = 850 \mu A \]
\[ R_0 = \frac{V_{OH}}{I_{ds}} = \frac{2.5}{850 \mu} = 2.94 k\Omega \]

$R_{mid}$:
\[ I_{ds} = \frac{k_n nW_n}{2 L_n} (V_{OH} - V_T)^2 (1 + \lambda V_M) = 795 \mu A \]
\[ R_{mid} = \frac{V_M}{I_{ds}} = \frac{1.27}{795 \mu} = 1.96 k\Omega \]

$R_{eq} = \frac{1}{2} (R_0 + R_{mid}) = 2.45 k\Omega$

Pull-up $R_{eq, pu}$:

$R_0$:
\[ I_{ds} = \frac{k_p pW_p}{2 L_p} (V_{DD} - V_{OL} - V_T)^2 (1 + \lambda (V_{DD} - V_{OL})) = 127 \mu A \]
\[ R_0 = \frac{(V_{DD} - V_{OL})}{I_{ds}} = \frac{2.5 - 0.242}{127 \mu} = 17.8 k\Omega \]

$R_{mid}$:
\[ I_{ds} = \frac{k_p pW_p}{2 L_p} (V_{DD} - V_{OL} - V_T)^2 (1 + \lambda (V_{DD} - V_M)) = 116 \mu A \]
\[ R_{mid} = \frac{(V_{DD} - V_M)}{I_{ds}} = \frac{2.5 - 1.27}{116 \mu} = 10.6 k\Omega \]

$R_{eq} = \frac{1}{2} (R_0 + R_{mid}) = 14.2 k\Omega$
$$t_{pHL} = 0.69 \, R_{eq\_pd} \, C_L = 169 \, \text{ps}$$
$$t_{pLH} = 0.69 \, R_{eq\_pu} \, C_L = 980 \, \text{ps}$$
$$t_p = 575 \, \text{ps}$$

**Inverter B**

**Pull-down \(R_{eq\_pd}\):**

\[ R_0: \]
\[
I_{ds} = \frac{k_n \, W_n}{2 \, L_n} (V_{OH} - V_T)^2 \left( 1 + \lambda V_{OH} \right) = 450 \mu A
\]
\[
R_0 = \frac{V_{OH}}{I_{ds}} = \frac{1.76}{450 \mu} = 3.9 \Omega
\]

\[ R_{mid}: \]
\[
I_{ds} = \frac{k_n \, W_n}{2 \, L_n} (V_{OH} - V_T)^2 \left( 1 + \lambda V_M \right) = 429 \mu A
\]
\[
R_{mid} = \frac{V_M}{I_{ds}} = \frac{.921}{429 \mu} = 2.2 \Omega
\]

\[
R_{eq} = \frac{1}{2} (R_0 + R_{mid}) = 3.1 \Omega
\]

**Pull-up \(R_{eq\_pu}\):**

\[ R_0: \]
\[
I_{ds} = \frac{k_n \, W_n}{2 \, L_n} (V_{DD} - V_{OL} - V_{T0} - \gamma \left( \sqrt{ V_{t0} + V_{OL} } - \sqrt{ V_{t0} + V_{OL} } \right)^2 \left( 1 + \lambda (V_{DD} - V_{OL}) \right) = 117 \mu A
\]
\[
R_0 = \frac{V_{DD} - V_{OL}}{I_{ds}} = 2.5 \frac{.226}{117 \mu} = 19.4 \Omega
\]

\[ R_{mid}: \]
\[
I_{ds} = \frac{k_n \, W_n}{2 \, L_n} (V_{DD} - V_{OL} - V_{T0} - \gamma \left( \sqrt{ V_{t0} + V_{OL} } - \sqrt{ V_{t0} + V_{OL} } \right)^2 \left( 1 + \lambda (V_{DD} - V_M) \right) = 113 \mu A
\]
\[
R_{mid} = \frac{V_{DD} - V_M}{I_{ds}} = 2.5 \frac{.921}{113 \mu} = 14 \Omega
\]

\[
R_{eq} = \frac{1}{2} (R_0 + R_{mid}) = 16.7 \Omega
\]
\[ t_{pHL} = 0.69 R_{eq_{pd}} C_L = 214 \text{ps} \]
\[ t_{pLH} = 0.69 R_{eq_{pu}} C_L = 1.15 \text{ns} \]
\[ t_p = 682 \text{ps} \]

**Inverter C**

**Pull-down \( R_{eq_{pd}} \):**

\[ R_0: \]
\[ I_{ds} = \frac{k_n}{2} \frac{W}{L_n} (V_{OH} - V_T)^2 (1 + \lambda V_{OH}) = 567 \mu A \]
\[ R_0 = \frac{V_{OH}}{I_{ds}} = 2.5 \frac{V}{567 \mu \Omega} = 4.41 \Omega \]

\[ R_{mid}: \]
\[ I_{ds} = \frac{k_n}{2} \frac{W}{L_n} (V_{OH} - V_T)^2 (1 + \lambda V_M) = 530 \mu A \]
\[ R_{mid} = \frac{V_M}{I_{ds}} = 1.25 \frac{V}{530 \mu \Omega} = 2.36 \Omega \]

\[ R_{eq} = \frac{1}{2} (R_0 + R_{mid}) = 3.39 \Omega \]

**Pull-up \( R_{eq_{pu}} \):**

\[ R_0: \]
\[ I_{ds} = \frac{k_p}{2} \frac{W}{L_p} (V_{DD} - V_{OL} - V_T)^2 (1 + \lambda (V_{DD} - V_{OL})) = 496 \mu A \]
\[ R_0 = \frac{(V_{DD} - V_{OL})}{I_{ds}} = 2.5 \frac{V}{496 \mu \Omega} = 5 \Omega \]

\[ R_{mid}: \]
\[ I_{ds} = \frac{k_p}{2} \frac{W}{L_p} (V_{DD} - V_{OL} - V_T)^2 (1 + \lambda (V_{DD} - V_M)) = 448 \mu A \]
\[ R_{mid} = \frac{(V_{DD} - V_M)}{I_{ds}} = 2.5 - 1.19 \frac{V}{448 \mu \Omega} = 2.9 \Omega \]

\[ R_{eq} = \frac{1}{2} (R_0 + R_{mid}) = 3.95 \Omega \]
Here’s the HSPICE file to generate curves for the inverters:

```plaintext
* EE141 SPRING 2005 HW2 PROB 4
.model nmos NMOS (LEVEL = 1
+ VTO = 0.5 KP = 18e-6 GAMMA = 0.5 LAMBDA = 0.06 PHI = 0.3)
.model pmos PMOS (LEVEL = 1
+ VTO = -0.5 KP = 5e-6 GAMMA = 0.5 LAMBDA = 0.1 PHI = 0.3)
*Inverter A
M1 vout_pn 0 vdd vdd pmos W=1u L=0.5u
M2 vout_pn vin 0 0 nmos W=1.5u L=0.5u
*Inverter B
M3 vdd vdd vout_n 0 nmos W=0.5u L=0.5u
M4 vout_n vin 0 0 nmos W=2.0u L=0.5u
*Inverter C
M5 vout_std vin vdd vdd pmos w=3u l=0.5u
M6 vout_std vin 0 0 nmos w=1u l=0.5u
*Sources
VSUPP vdd 0 2.5
.options post=2
.op
VSRC vin 0 pulse 0 2.5 0 100p 100p 1n 2n
.tran 500p 4ns
.END
```

Running this you’ll find that the measurements above for propagation delay are in the same order of magnitude as what HSPICE will give you, however, it’s clear that this approximation isn’t that accurate. Showing the HSPICE is good enough for this problem.

Here’s the HPSICE code for a ring oscillator (5 inverters of type C, inverters A and B can be constructed similarly):

```plaintext
* EE141 SPRING 2005 HW2 PROB 4c
.model nmos NMOS (LEVEL = 1
+ VTO = 0.5 KP = 18e-6 GAMMA = 0.5 LAMBDA = 0.06 PHI = 0.3)
.model pmos PMOS (LEVEL = 1
+ VTO = -0.5 KP = 5e-6 GAMMA = 0.5 LAMBDA = 0.1 PHI = 0.3)
*Inverter C
.subckt INV in out inv_vdd inv_gnd
  M5 out in inv_vdd inv_vdd pmos w=3u l=0.5u
.END
```
M6 out in inv_gnd inv_gnd nmos w=1u l=0.5u
.ends in

* use subckts
X1 vin com1 vdd 0 INV
X2 com1 com2 vdd 0 INV
X3 com2 com3 vdd 0 INV
X4 com3 com4 vdd 0 INV
X5 com4 vi
.ic V(vin)=0 V(com1)=2.5 V(com2)=0 V(com3)=2.5 V(com4)=0

*Sources
VSUPP vdd 0 2.5
.options post=2
.op
.tran 500p 4ns UIC
.END