PROBLEM 1. Logic Styles (14 points)

In this problem, we will implement a logic function $Y = (AB + C)D$. For single-ended logic styles, inputs with only one polarity are available, while for differential logic styles you can use both true and complementary inputs.

a) (2 pts) Implement the function $Y$ in standard complementary CMOS:

\[
\overline{Y} = \overline{(AB + C)} \overline{D}
\]

\[
Y = (A + \overline{B})\overline{C} + \overline{D}
\]

\[
\overline{Y} = \overline{A} \overline{B} \overline{C} \overline{D}
\]

b) (4 pts) Size the transistors in the gate implemented in a) such that it drives the output equivalently to a symmetrically-sized ($Wp/Wn = 2/1$) inverter.
c) (8 pts) Implement the function $Y$ in a differential, complementary pass-transistor logic family (NMOS transistors only should be used to implement the function).
PROBLEM 2. Logical Effort (18 points)

Consider two different implementations of an 8-bit decoder, driving the load 9 times larger than its input capacitance.

Design 1: Predecoder: NAND4 + INV, row decoder: NAND2 + INV.
Design 2: Predecoder: NAND2 + INV, row decoder: NAND4 + INV.

Assume γ=1. Fanout-of-4 inverter delay is 100ps.

a) (6 pts) Calculate the path effort of both designs, with all gates symmetrically sized.

\[ H_1 = \text{GBF} = 2 \cdot 1 \cdot \frac{4}{3} \cdot 1 \cdot 16 \cdot 8 \cdot 9 = 3072 \]

\[ H_2 = \text{GBF} = \frac{4}{3} \cdot 1 \cdot 2 \cdot 1 \cdot 2 \cdot 64 \cdot 9 = 3072 \]

**H_1 = 3072 \quad H_2 = 3072**
b) (6 pts) What is the propagation delay of each of the designs when the constituent gates are sized to minimize delay?

\[ t_{p_1} = t_{p_0} \left( \leq p_1 + 4 \sqrt[4]{H_1} \right) \]

\[ = t_{p_0} \left( 4 + 1 + 2 + 1 + 4 \cdot 7.444 \right) \]

\[ = 37.78 \ t_{p_0} \]

\[ t_{p_0} = 20 \ \text{ps} \]

\[ t_{p_1} = 756 \ \text{ps} \]

\[ H_1 = H_2 \ and \ p_1 \ are \ the \ same \ for \ both \ design. \]

\[ t_{p_2} = 756 \ \text{ps}. \]
c) (6 pts) Now assume that you would like to minimize the propagation delay only of the LH transition at the output. Each of the gates can be sized to have the LH and HL delays differ by a factor of 2. Size the Design 2 to minimize the LH delay. Calculate this propagation delay.

\[ t_p = t_{po} \left( \leq p_{i1} + 4 \cdot \sqrt{H} \right) \]

\[ = 20 \text{ps} \left( \frac{5}{6} + \frac{5}{6} + \frac{4}{3} + \frac{8}{3} + 24.17 \right) \]

\[ = 596.6 \text{ps} \]

\[ t_{p2} = 596.6 \text{ps} \]
PROBLEM 3. SRAM Design (18 points)
Your colleagues in EE130 came up with a CMOS process where the PMOS transistor has as good mobility as the NMOS. They propose an alternate SRAM cell design, as in Figure 1.

Figure 1.

a) (2 pts) Should the wordline WL, be active high or low? Briefly explain.

Active Low

When WL is 0, access transistors are on.
b) (8 pts) Draw the bitline peripheral circuitry that is appropriate for this cell – i.e. transistors that provide bitline preconditioning, enabling read and write operations and writing into a cell. Draw the sense amplifier as a symbol (no need for transistor schematics). Label all signals. You can complete the figure below that shows two cells in the bitline.
c) (4 pts) Consider an alternate SRAM cell in a standard CMOS process, shown in Figure 2. This cell has separate wordlines for read and write operation, RWL and WWL, a pair of write bitlines, and a single-ended read bitline RBL. $V_{DD} = 2.5V$.

![Diagram of SRAM cell with labels: RWL, WWL, VDD, M3, M4, M5, M1, M2, M6, M7, M8, RBL, and WBL.]

What sizing constraint (if any) determines the read stability of this cell? Concisely explain your answer.

**No.**

The storage node is connected to the gate of $M_8$ during read operation.
d) (4 pts) Determine the widths and lengths of all transistors that result in a cell with minimum size and guaranteed functionality. $V_{DD} = 2.5V$, $L_{min} = 0.24\mu m$, $W_{min} = 0.36\mu m$.

Since there is no READ constraint, $M_5$ and $M_1$ can be minimum size transistors.

We can write into the cell, if

$$\frac{(W_L)^2}{(W_T)^5} = 1.$$ 

Therefore, all transistors can be minimum size.