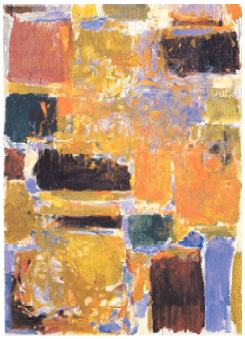
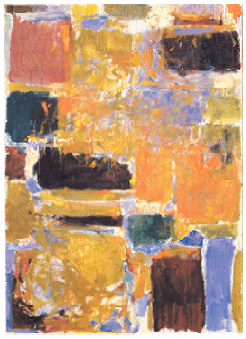


EE141-Spring 2006 Digital Integrated Circuits

Lecture 25
Clock Distribution
Power Distribution



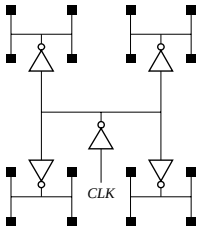
Clock Distribution

Administrative Stuff

- Homework #9 due this Thursday
- Visit to Intel, April 21
  - Signup sheet
  - Friday lab - project ph. 4 starts after we get back
- Project phase 4
  - Posted
  - In lab April 21-April 27
- Hardware lab this week
  - Friday section on April 28

Clock Distribution

H-tree

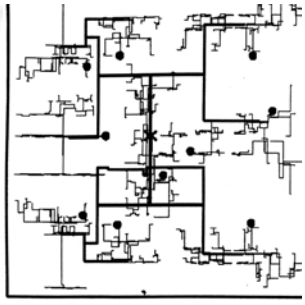


Clock is distributed in a tree-like fashion

Class Material

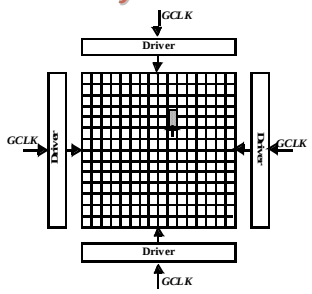
- Last lecture
  - Timing
- Today's lecture
  - Clock distribution
  - Power distribution
- Reading
  - Chapter 10, 9 (pp. 453-462, 469-475, 508-515)

More realistic H-tree



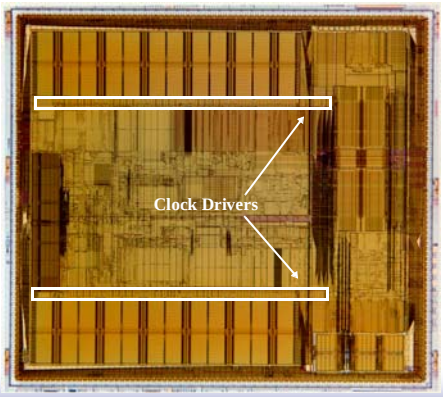
[Restle98]

The Grid System



- *No rc-matching*
- *Large power*

EECS141



EECS141

Example: DEC Alpha 21164

Clock Frequency: 300 MHz - 9.3 Million Transistors

Total Clock Load: 3.75 nF

Power in Clock Distribution network : 20 W (out of 50)

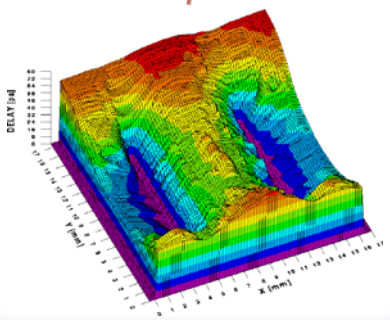
Uses Two Level Clock Distribution:

- **Single 6-stage driver at center of chip**
- **Secondary buffers drive left and right side clock grid in Metal3 and Metal4**

Total driver size: 58 cm!

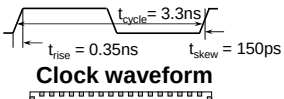
EECS141

Clock Skew in Alpha Processor

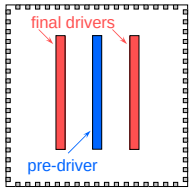


EECS141

21164 Clocking



Clock waveform

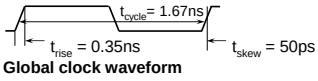


Location of clock driver on die

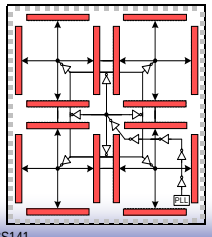
- 2 phase single wire clock, distributed globally
- 2 distributed driver channels
  - Reduced RC delay/skew
  - Improved thermal distribution
  - 3.75nF clock load
  - 58 cm final driver width
- Local inverters for latching
- Conditional clocks in caches to reduce power
- More complex race checking
- Device variation

EECS141

EV6 (Alpha 21264) Clocking 600 MHz – 0.35 micron CMOS



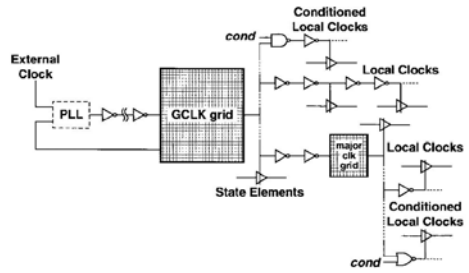
Global clock waveform



- 2 Phase, with multiple conditional buffered clocks
  - 2.8 nF clock load
  - 40 cm final driver width
- Local clocks can be gated “off” to save power
- Reduced load/skew
- Reduced thermal issues
- Multiple clocks complicate race checking

EECS141

21264 Clocking



EECS141

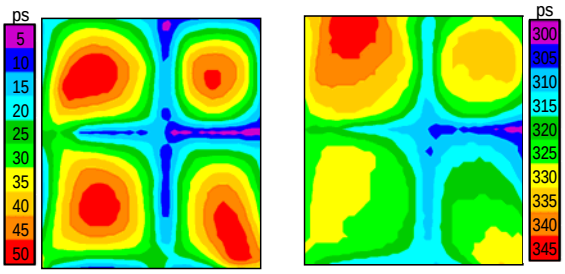
Clock Animations

- By Phillip Restle (IBM)

http://www.research.ibm.com/people/r/restle/Animations/DAC01top.html

EECS141

EV6 Clock Results



GCLK Skew
(at Vdd/2 Crossings)

GCLK Rise Times
(20% to 80% Extrapolated to 0% to 100%)

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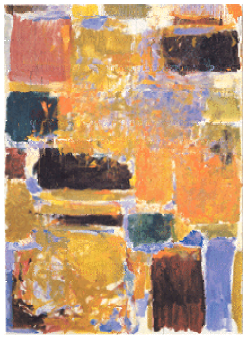
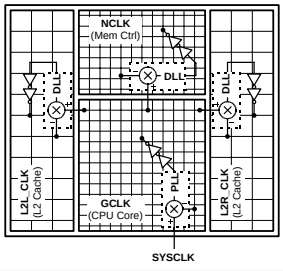


I/O Design

EECS141

EV7 Clock Hierarchy

Active Skew Management and Multiple Clock Domains



+ widely dispersed drivers
+ DLLs compensate static and low-frequency variation
+ divides design and verification effort
- DLL design and verification is added work
+ tailored clocks

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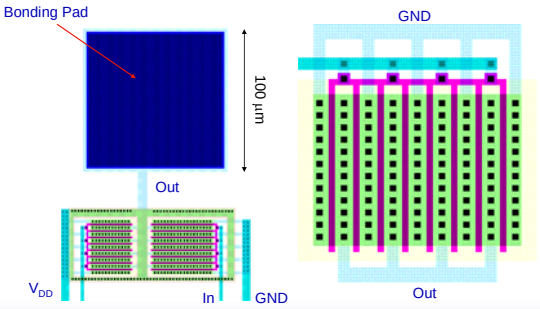
Bonding Pad Design



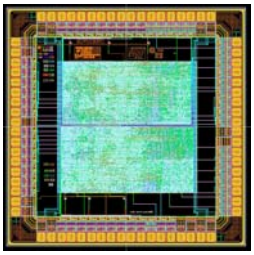
EECS141

ESD Protection

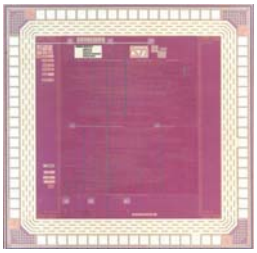
- When a chip is connected to a board, there is unknown (potentially large) static voltage difference
- Equalizing potentials requires (large) charge flow through the pads
- Diodes sink this charge into the substrate – need guard rings to pick it up.

Pad Frame

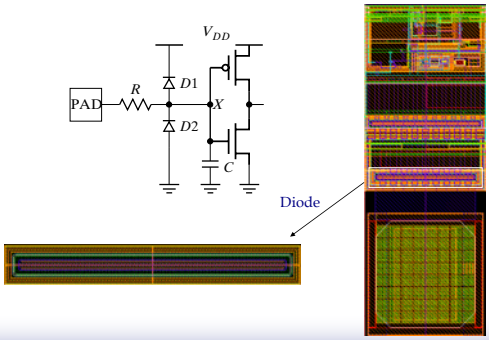
Layout



Die Photo

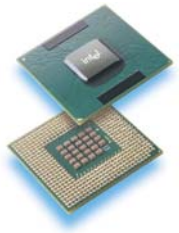


ESD Protection

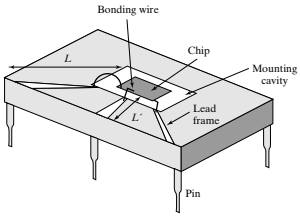


Chip Packaging

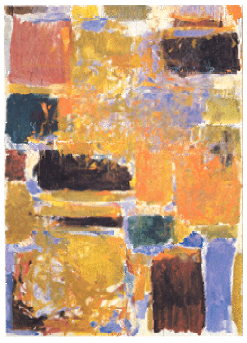
- An alternative is 'flip-chip':
  - Pads are distributed around the chip
  - The soldering balls are placed on pads
  - The chip is 'flipped' onto the package
  - Can have many more pads



Chip Packaging



- Bond wires (~25μm) are used to connect the package to the chip
- Pads are arranged in a frame around the chip
- Pads are relatively large (~100μm in 0.25μm technology), with large pitch (100μm)
- Many chips areas are 'pad limited'



Power Distribution

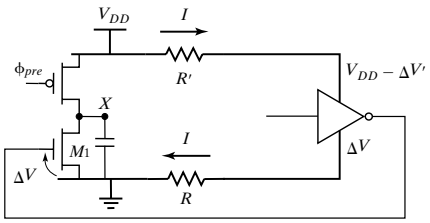
Impact of Resistance

- We have already learned how to drive RC interconnect
- Impact of resistance is commonly seen in power supply distribution:
  - IR drop
  - Voltage variations
- Power supply is distributed to minimize the IR drop and the change in current due to switching of gates

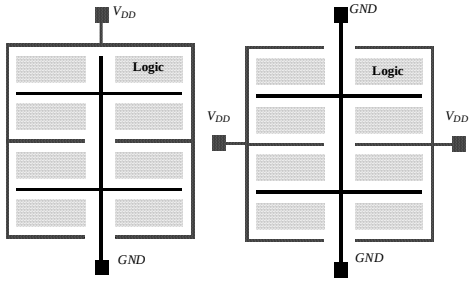
Power Distribution

- Low-level distribution is in Metal 1
- Power has to be 'strapped' in higher layers of metal.
- The spacing is set by IR drop, electromigration, inductive effects
- Always use multiple contacts on straps

RI Introduced Noise



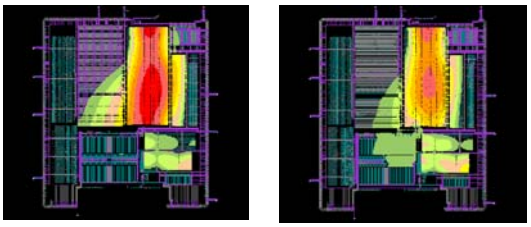
Power and Ground Distribution



(a) Finger-shaped network (b) Network with multiple supply pins

Resistance and the Power Distribution Problem

Before After



- **Requires fast and accurate peak current prediction**
- **Heavily influenced by packaging technology**

Source: Cadence

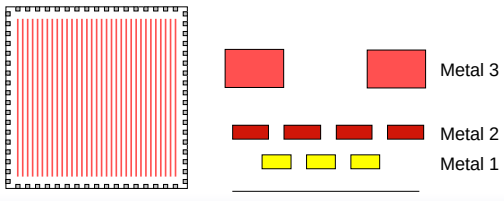
3 Metal Layer Approach (EV4)

3rd "coarse and thick" metal layer added to the technology for EV4 design

Power supplied from two sides of the die via 3rd metal layer

2nd metal layer used to form power grid

90% of 3rd metal layer used for power/clock routing

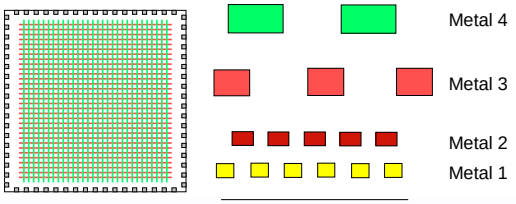


Courtesy Compaq

4 Metal Layers Approach (EV5)

4th "coarse and thick" metal layer added to the technology for EV5 design

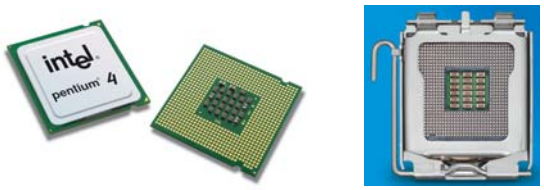
Power supplied from four sides of the die
Grid strapping done all in coarse metal
90% of 3rd and 4th metals used for power/clock routing



Courtesy Compaq

Decoupling Capacitors

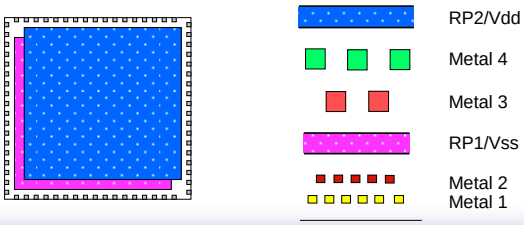
- Under the die



6 Metal Layer Approach – EV6

2 reference plane metal layers added to the technology for EV6 design

Solid planes dedicated to Vdd/Vss
Significantly lowers resistance of grid
Lowers on-chip inductance

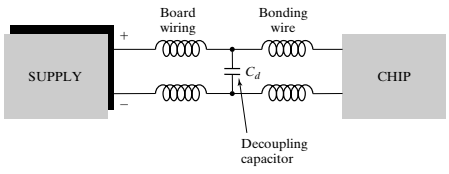


Courtesy Compaq

Next Lecture

- Adder design

Decoupling Capacitors



Decoupling capacitors are added:

- On the board (right under the supply pins)
- On the chip (under the supply straps, near large buffers)