Use the EECS240 0.18\(\mu\)m CMOS process in all home works and projects unless noted otherwise. In this homework you may use just the typical (tt) device parameters.

1. **Pole-Zero Doublets:** In this problem we will looking at the behavior of the circuit shown below in order to gain some intuition into the origin and response of pole-zero doublets.

   ![Circuit Diagram](image)

   a. Derive the transfer function \(H(s) = V_{out}(s)/V_{in}(s)\) of the circuit. What are the DC gain \((A_{vo})\), the location of the zero \((\omega_z)\), and the location of the pole \((\omega_p)\) as a function of \(R_1, R_2, C_1,\) and \(C_2\)?
   
   b. Now let’s look at the step response of this circuit. Immediately after the step is applied, what is the value of \(V_{out}\)?
   
   c. Derive an expression for \(V_{out}(t)\) when \(V_{in}(t)\) is a 1V step, and sketch these responses for two representative cases: (1) \(\omega_z > \omega_p\) and (2) \(\omega_p > \omega_z\). Hint: you do not need to perform any inverse Laplace transforms to get the analytical expression.
   
   d. For parts d. and e. of this problem, we will consider the following transfer function (with \(\omega_{p1}, \omega_{p2},\) and \(\omega_z\) all real and positive):

   \[
   H(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p_1(1 + s/\omega_p_2)}
   \]

   Sketch \(|H(j\omega)|\) as a function of \(\omega\) for (1) \(\omega_{p1} < \omega_z < \omega_{p2}\) and (2) \(\omega_{p1} < \omega_{p2} < \omega_z\).
   
   e. Sketch the time domain step response of \(H(s)\) for cases (1) and (2). Will the step response ever overshoot its final value in these two cases? Hint: you may want to find an \(H_1(s)\) and \(H_2(s)\) such that \(H(s) = c_1H_1(s) + c_2H_2(s)\). – i.e., you should use a partial fraction expansion.

2. **Switched-capacitor amplifier:** What is the total noise variance at the output of the switched capacitor amplifier shown below at the end of a complete cycle (i.e., during \(\phi_2\))? You can assume that the OTA is simply implemented by an NMOS common-source stage with a given \(g_m\) and infinite \(r_c\).

   ![Switched-capacitor Amplifier Diagram](image)
3. **Gain Boosted Cascode:** This problem will focus on the gain-boosted cascode amplifier shown below. To simplify the analysis, you can ignore the $r_e$ of the transistors and all of the capacitors except for those explicitly drawn in the diagram.

![Diagram of the gain-boosted cascode amplifier](image)

a. What is the frequency response $H(s) = \frac{v_3(s)}{v_1(s)}$ of this amplifier? Approximately what is the unity gain frequency of the amplifier?

b. Approximately what conditions are required to guarantee that the gain boosting feedback loop maintains at least 45° of phase margin? You should provide your answer in terms of $g_m1$, $g_m2$, $g_m3$, $R3$, $C1$, $C2$, and $C3$.

c. Assuming the current sources are ideal, what is the total noise variance at the output of the amplifier? An approximate answer will receive full credit, but for bonus points you can solve for the impact of all of the noise sources. You may find partial fraction expansions handy to avoid the need to do any additional frequency response integrations beyond the first and second order ones provided in the lecture notes.