In this second and final phase of the project, we will be exploring the design of a complete analog front-end for a high-speed serial link. Below is a conceptual schematic highlighting the main components of the front-end.

Once again, you will not be provided with a set of specifications on each of the components – figuring out the right specifications and tradeoffs is an integral part of the project. In fact, for this project we will not even specify the target data-rate. Rather, as long as your data-rate is above the minimum required (2 Gb/s), you are free to explore the tradeoffs between data-rate and power consumption. However, no matter what data-rate you choose, you should be sure to minimize the circuit power required to achieve this data-rate.

The primary component you will need to design for this project is the receiver amplifier/equalizer; SPICE netlists for a transmitter and a comparator have been posted on the course web-site. Note however that you are by no means constrained to work only the equalizer – as long as your link functions correctly and meets the constraints provided below, you are free to modify any of the circuit components as you see fit. Note however that each one of the components has a nearly infinite number of different possible implementations, so don’t just randomly tinker with the various elements. Instead, you should be sure to analyze which elements appear to be the most critical and will provide you the highest “return on investment” for the time you spend on them.

Instead of arbitrarily fixing the offsets of each of the components (e.g., the comparator) like in phase I of the project, we will be assuming that the offsets in our fully differential structures are dominated by threshold voltage mismatch. Thus, you will be using Pelgrom’s model to calculate the $\sigma$ of threshold voltage mismatch between each pair of matched transistors. Since we want high yield, we will be assuming a worst-case mismatch of $3\sigma$.

The specifications and constraints for your design are:

- Process: EE240 0.18 µm CMOS, tt corner
  - $A_{Vth} = 8 \text{ mV} \cdot \mu\text{m}$
- Operating temperature: 25°C
- Data-rate: $>2$ Gb/s over either of the two channels (see below)
- BER: $< 10^{-15}$ with worst-case mismatch of $3\sigma$ for each pair of matched transistors
- Maximum input capacitance on $d_i$, $d_i_b$: 50 fF
- Capacitive load on data outputs: 50 fF
- Current mirror ratios: $\leq 20$
Some additional notes and guidelines:

- You can use a total of two ideal current sources in your design: one for the transmitter, one for the receiver. Any current source loads in your signal path must be implemented with real transistors.
- You can use a maximum of 3 independent power supplies in your design (as indicated in the figure above): $V_{T_{,TX}}$, $V_{T_{,RX}}$, and $V_{DD}$. Each of these supplies can take any value you’d like them to.
- You are allowed to use ideal resistors, but any capacitors in your circuit must be implemented out of MOS devices or MOM structures. For MOM capacitors, you can use the parameters of either vertical or horizontal parallel plates from HW#1.
- Don’t forget to include the source and drain perimeters and areas for each of your devices, or to implement common-mode feedback if it is required.
- The “default” transmitter which has been provided to you in “tx.sp” is a “current-mode” design that is scalable in terms of the swing it provides at the output. For example, if you instantiate the transmitter with:

  xtx di di_b vp_t vn_t vdd tx sw=0.1

then the swing at the output of the transmitter will have 100 mV of differential amplitude (i.e., 200 mV peak-to-peak). If you are unsure what swing to pick, start with 100 mV.
- Your link must function correctly over two different channels: “chan1.sp” and “chan2.sp” – both of which have posted on the course website. You can use as many digital control bits as you’d like to program the response of your equalizer. When quoting your data-rate, note that you must achieve this data-rate on both of these channels. i.e., if you can run your link at 5 Gb/s on one channel, but only 2 Gb/s on the other, you should quote your data-rate as 2 Gb/s.
- You can also use as many digital bits as you’d like to implement offset correction circuitry.
- You can place your sampling clock anywhere within the data eye you’d like, as long as it is always at the same relative time within the bit. You can also use as many clock phases as you’d like. However, your clocks must be driven by real inverters, and you must include the power dissipated by these inverters when calculating your total power consumption.
- Although you will not explicitly include common-mode or power-supply noise in your simulations or BER calculations, you will need to characterize the sensitivity of your receiver to common-mode and power-supply variations. Further details on setting these simulations up will be provided in lecture.

Your final submission for the project will consist of two parts: 1) a written report including the items listed below, and 2) a 2 minute, 3 slide presentation about your design that you will give during lecture on the final day of class (May 8th). (Your presentation will not be recorded.)

The written report should include:

1. A brief summary of the specifications you achieved (all for the worst-case channel):
   - Data-rate:
   - Total power consumption:
     - TX:
     - Equalizer:
     - Comparator:
   - Worst-case BER:
     - Min. eye opening at RX input:
     - Total offset at comparator input:
     - Total noise at comparator input:
   - Robustness
     - RX CM to DM gain at DC:
     - RX CM to DM gain at worst-case frequency:
     - RX power supply to DM gain at DC:
     - RX power supply to DM gain at worst-case frequency:
2. **Clearly** labeled schematics of any new components you designed, including device sizes and nominal bias currents. (You do not need to show the transmitter or comparator if you simply used the default designs.)

3. A **concise, clear** description of the procedure you followed to design the front-end. Some example questions you should aim to answer include: What were your main goals? (e.g., highest speed or lowest power) How did you decide upon the equalizer topology? If you modified other components, how did you choose which ones to modify? How did you set your swing at the transmitter?

4. Hand analysis and simulations plots/printouts verifying that your design meets the specifications your provided in 1. In addition, you should provide plots from the simulations you ran to characterize the common-mode/power-supply sensitivity of your design.

5. An electronic text or Excel file listing the simulated differential voltage at the input of your comparator and the digital output of the comparator vs. time for the data inputs provided in `eye_input_full.sp` (which will be posted on the course web-site).

6. The HSPICE netlist of your design (again, you do not need to include any of the “default” components you used).