You should write your results on the exam sheets only. Partial credit will be given only if you show your work and reasoning clearly.

Throughout the exam, you can ignore the $r_o$ of any transistors and all capacitors except those explicitly drawn in the diagrams unless the problem states otherwise.

Name: _______________________________

SID: ________________________________

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Problem 1 (16 points) Active Inductors

a) (4 pts) As we will explore further in this problem, many of the equalizers discussed in class make use of so-called “active inductors”. For what values of $R_{eq}$ and $L_{eq}$ will the $Z_{in}$’s of the two circuits shown below exactly equal each other? You should provide your answer in terms of the $g_{m}$ of the transistor and $\omega_z = (R_zC_z)^{-1}$. You should assume that the unity-gain buffer in the active inductor is ideal (i.e., has infinite input impedance and zero output impedance).

$$Z_{in} = R_{eq} + sL_{eq}$$

So:

$$R_{eq} = \frac{1}{g_m}$$

$$L_{eq} = \frac{1}{g_m\omega_z}$$

b) (2 pts) Given your answer to part a), if $g_m = 500\mu S$, what value of $L_{eq}$ is required for $\omega_z$ to equal $2\pi \cdot 200\text{MHz}$?

$$L_{eq} = \frac{1}{500\mu S \cdot 2\pi \cdot 200\text{MHz}}$$

$$L_{eq} = 1.59 \mu H$$ (Note that this is huge for an on-chip inductor)
c) **(4 pts)** For the equalizing amplifier shown below, what is the variance of the noise at $V_{\text{out}}$ due only to the thermal noise of $R_L$? (i.e., you can ignore the noise from the input transistor) You should provide your answer in terms of $kT$, $C_L$, $L_{\text{eq}}$, and $R_L$.

\[
\frac{V_{\text{out}}}{V_N} = \frac{1}{\frac{1}{8} C_L + \frac{1}{R_L} + 6L_{\text{eq}}} = \frac{1}{\frac{5}{8} R_L C_L + 3R_L C_L + 1}
\]

\[
\sum_{0}^{\infty} \frac{V_{\text{out}}^2(f)}{V_N^2} df = \frac{1}{4R_L C_L}
\]

\[
\sigma_{V_{\text{out}}}^2 = V_N^2 \cdot \frac{1}{4R_L C_L} = 4kT R_L \cdot \frac{1}{4R_L C_L}
\]

\[
\sigma_{V_{\text{out}}}^2 = \frac{kT}{C_L}
\]
d) (6 pts) What is the noise variance at $V_{out}$ due only to the thermal noise of the load for the active inductor equalizer shown below? You can ignore the noise from $R_z$, but note that there is no longer a buffer isolating $R_z$ and $C_z$ from the output (i.e., you should include the loading due to $R_z$ and $C_z$). You should provide your answer in terms of $kT$, $\gamma$, $\omega_z$, $C_L$, and $C_z$.

$$Z_L = \frac{1}{sC_L} \left| \frac{(1+sR_2C_z)}{sC_z} \left| \frac{(1+sR_2C_z)}{g_m} \right. \right.$$  

$$Z_L = \frac{1}{sC_L} \left| \frac{(1+s/w_2)^2}{g_m(1+s/w_2) + sC_2(1-s/w_2)} \right.$$  

$$Z_L = \frac{1}{sC_L} \left| \frac{(1+s/w_2)}{g_m + sC_2} = \frac{(1+s/w_2)}{g_m + sC_2 + sC_L + s^2C_L/w_2} \right.$$  

$$Z_L = \frac{1}{g_m} \cdot \frac{s^2C_L/g_mw_2 + s(C_L+C_2)}{g_m} + 1$$  

$$\int \! \|Z_L\|^2 \, db = \frac{1}{g_m^2} \cdot \frac{g_m}{4(C_L+C_2)} \cdot \left( \frac{g_mw_2}{C_Lw_2^2} + 1 \right)$$  

$$\sigma^2_{V_{out}} = 4kT \cdot g_m \cdot \frac{1}{g_m} \cdot \frac{1}{4(C_L+C_2)} \cdot \left( \frac{g_m/C_L}{w_2} + 1 \right)$$  

$$\sigma^2_{V_{out}} = \frac{kT}{(C_L+C_2)} \cdot \gamma \left( \frac{1 - g_m/C_L}{w_2} \right)$$

(Note that if $C_2 \gg C_L$ and $g_mR_z \gg 1$, $\sigma^2_{V_{out}}$ can be simplified to $\frac{kT}{C_L} \cdot \gamma \cdot g_mR_z$)
Problem 2 (16 points) Equalizer Design

This problem will examine the link shown below, where the channel behaves as a single-pole low-pass filter, and the receiver uses the R1/R2/C1 network to perform equalization. You can assume that the amplifier in the receiver has zero output impedance.

\[ \frac{V_{out}}{V_a} = \frac{R_2}{R_2 + \frac{1}{(1 + s/\omega_{chan})}} = \frac{R_2}{\frac{1}{R_1 C_1}} = \frac{R_2 (1 + s R_1 C_1)}{R_1 R_2 C_1 + R_1 + R_2} = \frac{R_2}{R_1 - R_2} \cdot \frac{(1 + s R_1 C_1)}{R_1 (1 + R_2 C_1)} \]

Zero: \( w_z = \frac{1}{R_1 C_1} \rightarrow C_1 = \frac{1}{R_1 w_{chan}} \)

Pole: \( \frac{R_1 R_2 C_1}{R_1 - R_2} = \frac{1}{w_{bit-rate}} \)

\[ \frac{R_2}{R_1 - R_2} \cdot \frac{1}{R_1} \cdot \frac{1}{w_{chan}} = \frac{1}{w_{bit-rate}} \]

\[ \frac{R_2}{R_1 + R_2} = \frac{w_{chan}}{w_{bit-rate}} \] (DC gain)

\[ (1 - \frac{w_{chan}}{w_{bit-rate}}) R_2 = \frac{w_{chan}}{w_{bit-rate}} R_1 \]

\[ R_2 = \frac{w_{chan}}{w_{bit-rate} - w_{chan}} \cdot R_1 \]
b) (4 pts) Given your answer to a), if we’d like the overall gain (i.e., $|V_{out}/V_{in}|$) of the equalizer to be equal to $A_{eq}$ over a 3dB bandwidth of $\omega_{bit\_rate}$, what is the total gain-bandwidth required of the amplifier? You should provide your answer in terms of $A_{eq}$, $\omega_{chan}$, and $\omega_{bit\_rate}$.

DC gain of RC network = \frac{\omega_{chan}}{\omega_{bit\_rate}}

So, amplifier needs $A_{eq} \cdot \frac{\omega_{bit\_rate}}{\omega_{chan}}$ of gain, and bandwidth of $\omega_{bit\_rate}$.

\Rightarrow \text{Gain-bandwidth} = A_{eq} \cdot \frac{\omega_{bit\_rate}^2}{\omega_{chan}}
c) (4 pts) Now let’s assume that due to a design error, both the zero and the DC gain of the equalizer are 3 times lower than their expected values. Ignoring the finite bandwidth of the amplifier, sketch the new equalized response in the frequency domain (i.e., $||V_{out}(j\omega)/V_{tx}(j\omega)||$). Be sure to label the magnitudes and frequencies of all relevant break-points.

![Graphs showing equalized response](image)

d) (4 pts) For the situation in c), how much smaller is the worst-case eye opening in comparison to the case where R1 takes on the correct value? (Hint: Sketch the step response of $V_{out}/V_{tx}$)

The step response overshoots and then goes back to the DC gain:

![Step response graph](image)

Worst case eye is 3 times smaller than if both zero & DC gain were in right place.
Problem 3 (20 points) CML Latch

In this problem we will be looking at the CML latch shown below. M1, M2, M3, and M4 all have a channel length of 0.2µm and the same width. The widths of these devices are chosen to achieve a fixed $V^*$ of 200mV. M5 and M6 are operated as switches that you can assume are ideal.

Unless otherwise noted, you should use the following design and technology parameters:
- $R_L = 2k\Omega$
- $I_b = 250\mu A$
- For $V^* = 200mV$, $I_{DS/W} = 25\mu A/\mu m$.
- $V_{DD} = 1.8V$
- $A_{Vth} = 8mV\cdot\mu m$
- $A_\beta = 4%\cdot\mu m$

a) (3 pts) What is the gain from $V_i$ to $V_o$ while M5 is on and M6 is off?

\[
I_b = 250\mu A \rightarrow 125\mu A / \text{device}
\]

\[
g_m = \frac{2I_0}{2V^*} = \frac{2 \cdot 125\mu A}{200mV} = 1.25 mS
\]

\[
A_V = g_mR_L = 1.25 mS \cdot 2k\Omega
\]

\boxed{A_V = 2.5}
b) **(4 pts)** What is the standard deviation (σ) of the input-referred offset of the latch due only to M1 and M2? Don’t forget to include the impact of β mismatch.

\[
W = \frac{125 \mu A}{25 \mu A/\mu m} \rightarrow W = 5 \mu m
\]

\[
\sigma^2_{offset} = \sigma^2_{\Delta V_{th}} + \sigma^2_{\Delta \beta/\beta} \left( \frac{I_0}{g_m} \right)^2
\]

\[
= \left( \frac{8 \mu V}{\mu m} \right)^2 + \frac{(490 \mu m)^2}{5 \mu m \cdot 0.2 \mu m} \cdot \left( \frac{\sqrt{2}}{2} \right)^2
\]

\[
= (8 \mu V)^2 + (4 \mu V)^2
\]

\[
\sigma_{offset} = 8.9 \mu V
\]

c) **(6 pts)** Given your answers to parts a) and b), what is the total σ of the input-referred offset of the latch? (Note that you can assume that the resistors are perfectly matched, but don’t forget to include the impact of M3 and M4.)

At \( V_o \), M3 and M4 have same \( \sigma_{offset} \) as M1 and M2 do at \( V_i \). So, total offset at \( V_i \) is:

\[
\sigma^2_{offset, tot} = \sigma^2_{offset, M1/M2} + \frac{\sigma^2_{offset, M3/M4}}{A_v^2}
\]

\[
\sigma^2_{offset, tot} = 92.8 \mu V^2
\]

\[
\sigma_{offset, tot} = 9.6 \mu V
\]
d) (4 pts) Assuming your answer to part c) was $\sigma_{\text{offset}}=10\text{mV}$, how much power would the latch need to dissipate in order to reduce the $\sigma_{\text{offset}}$ to 2mV? As you resize the latch to reduce the offset, you should maintain the same $V^*=200\text{mV}$ for all of the devices, as well as the same bandwidth and regeneration time constant (remember that the gate capacitors of M3 and M4 will load the output).

For fixed $V^*, W$ $\Rightarrow$ $I_b$

$L \Rightarrow C_g \alpha I_b$

$L \Rightarrow$ To keep bandwidth fixed, $R_L \propto \frac{1}{I_b}$

So, to get from $\sigma_{\text{offset}}=10\text{mV}$ to 2mV, need to increase device width by $(\frac{10\text{mV}}{2\text{mV}})^2 = 25$.

$I_{b,\text{new}} = 25 \cdot I_{b,\text{old}} = 6.3\text{mA}$

$P_{\text{new}} = 1.8\text{V} \cdot 6.3\text{mA}$

$P_{\text{new}} = 11.3\text{mW}$
e) (3 pts) Now returning to the original latch design with \( I_b = 250 \mu A \) and still assuming that the answer to part c) was \( \sigma_{\text{offset}} = 10 \text{mV} \), let’s consider the power required to cancel the offset of the latch using the programmable current trim circuit shown below. What is the maximum value of \( I_{\text{off+}} \) or \( I_{\text{off-}} \) required to cancel \( 3\sigma \) (i.e., \( 30 \text{mV} \)) of input-referred offset?

\[
\begin{align*}
V_{\text{off}} \text{ at input becomes } &g_m V_{\text{off}} \text{ of current at output.} \\
S_0, \quad I_{\text{off, max}} = g_m 3V_{\text{off}} = 1.25 \text{mA} \cdot 30 \text{mV} \\
&\boxed{I_{\text{off, max}} = 37.5 \mu A} \\
\text{(Way lower power than increasing device size!)}
\end{align*}
\]
Problem 4 (20 points) Miscellaneous

a) (6 pts) What is the small-signal loop gain $T(s)$ of the common-mode feedback loop shown below? You can assume that the OTA has a finite transconductance of $G_m$, but otherwise is ideal (i.e., it has infinite input and output impedance).

Break loop at input of OTA:

$$v_p = \frac{G_m}{sC_c} \cdot v_i \quad u_o = -2g_{mp} v_p \cdot R_m$$

$$T(s) = \frac{-G_m}{sC_c} \cdot 2g_{mp} R_m$$
b) **(6 pts)** In order to save power by turning on their biasing circuitry for only 10ns every 100us, one of your colleagues suggests augmenting their current mirrors with a sampling switch as shown below. What will likely be the largest source of error in the output current caused by this approach? What design steps could you take to mitigate this error? (Two correctly explained suggestions will receive full credit on this problem.)

* Biggest likely source of error is charge injection.

* Wors is a long time, so especially in a modern process, leakage could also be a problem.

* Both issues improve if \( C_s \) is increased.

\[
\Delta V_{\text{charge-inj}} = \frac{Q_{\text{inj}}}{C_s}, \quad \text{and} \quad \Delta V_{\text{leak}} = \frac{I_{\text{leak}} \cdot t_{\text{hold}}}{C_s}.
\]

* This circuit isn’t differential, so even fined portion of charge injection is problematic.

Most straightforward partial remedy is a dummy switch. (Note that bottom-plate sampling doesn’t really help this.)
c) **(8 pts)** Shown below is a two-stage Miller compensated amplifier tied in unity-gain feedback along with its bias generation circuit. How can you modify the bias circuit to ensure that the closed-loop bandwidth of the amplifier remains constant across process, voltage, and temperature variations? (Hint: What reference source might be available that is measured in the same units as bandwidth?) To receive full credit on this problem, you should describe the relationships that set the closed-loop bandwidth of your modified circuit.

* Bandwidth has units of frequency - use a constant frequency to generate the reference.
* Bandwidth set by \( \frac{g_m}{C_c} \), where \( C_c \) is a MOS cap. So, want \( g_m \cdot \frac{1}{f_{ref}} \cdot C_{mus} \)
* For "constant gm" reference circuit, \( g_m \cdot \frac{1}{R} \) \( \Rightarrow \) So, want \( g_m \cdot \frac{1}{R} \cdot \frac{1}{f_{ref}} \cdot C_{mus} \)
* \( \rightarrow \) switched cap \( R \)!
New bias circuit:

\[ R \propto \frac{1}{f_{\text{ref}} C_{\text{ref}}} \rightarrow g_{\text{m}} \frac{f_{\text{ref}} C_{\text{ref}}}{C_{\text{e}}} \]

\[ \text{Bandwidth} \propto f_{\text{ref}} \cdot \frac{C_{\text{ref}}}{C_{\text{e}}} \]

PMOS to match $C_e$

(Might add more cap at $V_s$ to filter switching transients)