1. Design an NMOS common-source stage driving a 1pF load with 500MHz unity-gain bandwidth. Choose a sufficiently long L to achieve an open-loop gain of at least 30 for output voltages between 0.3V and 0.9V and minimize the power dissipation of the circuit. Determine the device width and bias current, and verify the gain and bandwidth with SPICE. Also, plot the small-signal gain $\frac{dV_o}{dV_i}$ as a function of the output DC level.

2. Integrate the input referred flicker noise of a 1/0.09 NMOS transistor in a common-source configuration from 1Hz to 2GHz. Specify the result in Volts rms. Use $V^* = 150$mV, $g_m = 5\mu$S, $C_{ox} = 17$fF/$\mu$m$^2$, and the $K_f$ parameters from the lecture notes. How does the result change if you reduce the lower limit of integration to 1 day$^{-1}$? Find the factor $M$ by which $W$ and $I_D$ must be increased (keeping $g_m/I_D$ constant) to accommodate the lower integration limit without an increase of the total noise.

3. Derive an expression for the input referred noise of an NMOS common-source amplifier $M_1$ with PMOS load $M_2$. Assume $M_1$ and $M_2$ are both in saturation and that a capacitor $C_L$ dominates the load at the output. Specify the result as the noise from $M_1$ multiplied by a factor that is a function of the $V^*$ of the two transistors. What does this imply about the $V^*$ you should choose for $M_1$ vs. $M_2$? You can neglect flicker noise for this analysis.

4. In this problem we will be working with the circuit shown below. You can assume that the transistors are saturated and ignore flicker noise for this problem.

![Circuit Diagram]

a) Ignoring all capacitors and the switch (i.e., assuming the switch is always on), calculate the voltage noise density at the output ($V_{out}$) due to the current noise from $M_1$. You should include the $r_o$ of both of the transistors.
b) Repeat part a), but now find the voltage noise density at the output due to the current noise from M2.

c) Using your results from parts a) and b), calculate the ratio of thermal noise contributed by M2 relative to the thermal noise due to M1. In order to simplify the expression, you can assume that $g_{m2}r_{o2} >> 1$. Based on this expression, comment on how the DC biasing of M2 affects its contribution to the thermal noise at the output.

d) Now calculate the noise sampled on $C_L$ when switch S1 is abruptly turned off after being on for a long period of time. You can assume that the current source is ideal (i.e., is noiseless) and that all capacitors except for $C_L$ and $C_p$ are negligible. For this part of the problem you can assume that the output resistance of the transistors is infinite.