Today’s Lecture

- EE240 CMOS Technology

- Passive devices
  - Motivation
  - Resistors
  - Capacitors
  - (Inductors)

- Next time: MOS transistor modeling
EE240 Process

- 90nm 1P7M CMOS
  - Minimum channel length: 90nm
  - 1 level of polysilicon
  - 7 levels of metal (Cu)
  - 1.2V supply
  - Models for this process not “real”

- Other processes you might see
  - Shorter channel length (45nm / 1V)
  - Bipolar, SiGe HBT
  - SOI

Process Options

- Available for many processes

- Add features to “baseline process”

  - E.g.
    - Silicide block option
    - “High voltage” devices (2.5V & 3.3V, >10V)
    - Low $V_{TH}$ devices
    - Capacitor option (2 level poly, MIM)
    - …
CMOS Cross Section

- Metal
- p⁻ substrate
- p⁺ diffusion
- Poly
- n⁻ well
- n⁺ diffusion

Dimensions

- 1.4nm
- 50nm
- 700µm
- ≥90nm
- 0.6µm
Why Talk About Passives?

Resistors

- No provisions in standard CMOS
- Resistors are bad for digital circuits →
  - Minimized in standard CMOS
  - But, often want big, well-controlled R for analog…
- Sheet resistance of available layers:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sheet resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>60 mΩ/□</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>5 Ω/□</td>
</tr>
<tr>
<td>N+/P+ diffusion</td>
<td>5 Ω/□</td>
</tr>
<tr>
<td>N-well</td>
<td>1 kΩ/□</td>
</tr>
</tbody>
</table>
How about an N-Well Resistor?

Silicide Block Option

<table>
<thead>
<tr>
<th>Layer</th>
<th>$R/\Omega$</th>
<th>$T_C$ [ppm/°C]</th>
<th>$V_C$ [ppm/V]</th>
<th>$B_C$ [ppm/V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>N+ poly</td>
<td>100</td>
<td>-800</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>P+ poly</td>
<td>180</td>
<td>200</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>N+ diffusion</td>
<td>50</td>
<td>1500</td>
<td>500</td>
<td>-500</td>
</tr>
<tr>
<td>P+ diffusion</td>
<td>100</td>
<td>1600</td>
<td>500</td>
<td>-500</td>
</tr>
<tr>
<td>N-well</td>
<td>1000</td>
<td>-1500</td>
<td>20,000</td>
<td>30,000</td>
</tr>
</tbody>
</table>

- Non-silicided layers have significantly larger sheet resistance
- Resistor nonidealities:
  - Temperature coefficient: $R = f(T)$
  - Voltage coefficient: $R = f(V)$
  - Manufacturing Variations
Resistor Example

Goal: \( R = 100 \, k\Omega, \, T_C = 1/R \times dR/dT = 0 \)

Example Solution: N+ and P+ poly resistors in series

\[
R = R_N (1 + T_{CN} \Delta T) + R_P (1 + T_{CP} \Delta T) \\
= \frac{R_N + R_P}{T_C} + \frac{R_N T_{CN} + R_P T_{CP}}{T_C} \Delta T \\
\Rightarrow
\]

\[
R_N = R \left( \frac{1}{T_C} \right) = 20k\Omega = 200 \text{ squares}
\]

\[
R_P = R \left( \frac{1}{T_C} \right) = 80k\Omega = 444.4 \text{ squares}
\]

Voltage Dependence
Voltage Coefficient

Example:
Diffusion resistor

\[ R = \frac{V_1 - V_2}{I} \]
\[ \approx R_c \left[ 1 + T_c \left( T - 25^\circ \right) + V_c \left( V_1 - V_2 \right) + B_c \left( \frac{V_1 + V_2}{2} - V_a \right) \right] \]

Resistor Matching

- Types of mismatch:
  - Run-to-run variations
    - Global differences in thickness, doping, etc.
  - Systematic (e.g. contacts)
  - Random variations between devices
- Run-to-run variations in absolute R value: 20+%
  - Can be problematic for termination, bias current, etc.
- Best case: make circuit depend only on ratios
  - E.g., use feedback to control opamp gain
  - With careful layout, can get 0.1 – 1% matching
Systematic Variations from Layout

- Example:
  
  ![Diagram showing R and 2R with variations from layout]

- Use unit element instead:
  
  ![Diagram showing use of unit element instead of R]

Common Centroid and Dummies

Example: \( R1 : R2 = 1 : 2 \)

- Dummy \( \rightarrow \) \( 0.5 \times R2 + \Delta R \)
- \( 0.5 \times R2 - \Delta R \)
- \( R1 \)
- Dummy \( \rightarrow \)
Resistor Layout (cont.)

Serpentine layout for large values:

Better layout (mitigates offset due to thermoelectric effects):


MOSFETs as Resistors

- **Triode region (“square law”):**
  \[
  I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} \quad \text{for} \quad V_{GS} - V_{TH} > V_{DS}
  \]

- **Small signal resistance:**
  \[
  \frac{1}{R} = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})
  \]
  \[
  R = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \quad \text{for} \quad V_{GS} - V_{TH} >> V_{DS}
  \]

- **Voltage coefficient:**
  \[
  V_C = \frac{1}{R} \frac{\partial R}{\partial V_{DS}} = \frac{1}{V_{GS} - V_{TH} - V_{DS}}
  \]
MOS Resistors

**Example:** \( R = 1 \text{ M} \Omega \)

- Large \( R \)-values realizable in small area
- Very large voltage coefficient

**Applications:**
- **MOSFET-C filters:** (linearization)
- **Biasing:** (>1G \( \Omega \))

\[
R = \frac{1}{\mu C_{ox} \cdot \frac{W}{L} (V_{gs} - V_{th})}
\]

\[
W = \mu C_{ox} R(V_{gs} - V_{th})
\]

\[
L = \frac{1}{100 \mu A/V^2 \times 1 \text{M} \Omega \times 2V} = \frac{1}{200}
\]

\[
V_c \bigg|_{V_{gs}=V_{th}} = \frac{1}{V_{gs} - V_{th}}
\]

\[
= \frac{1}{2V} = 0.5V^{-1}
\]

Resistor Summary

- No or limited support in standard CMOS
  - Large area (compared to FETs)
  - Nonidealities:
    - Large run-to-run variations
    - Temperature coefficient
    - Voltage coefficients (nonlinear)

- Avoid them when you can
  - Especially in critical areas, e.g.
    - Amplifier feedback networks
    - Electronic filters
    - A/D converters
  - We will get back to this point
Capacitors

• Simplest capacitor:


substrate

• What’s the problem with this?

Capacitors

• “Improved” capacitor:


substrate

• Is this only 1 capacitor?
### Capacitor Options

<table>
<thead>
<tr>
<th>Type</th>
<th>C [aF/μm²]</th>
<th>$V_C$ [ppm/V]</th>
<th>$T_C$ [ppm/°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate</td>
<td>10,000</td>
<td>Huge</td>
<td>Big</td>
</tr>
<tr>
<td>Poly-poly (option)</td>
<td>1000</td>
<td>10</td>
<td>25</td>
</tr>
<tr>
<td>Metal-metal</td>
<td>50</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>Metal-substrate</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal-poly</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Poly-substrate</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction caps</td>
<td>~1000</td>
<td>Big</td>
<td>Big</td>
</tr>
</tbody>
</table>

### MOS Capacitor

- High capacitance in inversion

- **SPICE:**

$$C = \frac{I}{\omega V}$$

$$V = 1V$$

$$\omega = I$$

$$\Rightarrow C = I$$
MOS Capacitor

- High non-linearity, temperature coefficient
- But, still useful in many applications, e.g.:
  - (Miller) compensation capacitor
  - Bypass capacitor (supply, bias)

Capacitor Layout

- Unit elements
- Shields:
  - Etching
  - Fringing fields
- “Common-centroid”
- Wiring and interconnect parasitics

MIM Capacitors

- Some processes have MIM cap as add-on option
  - Separation between metals is much thinner
  - Higher density

- Used to be fairly popular
  - But not as popular now that have many metal layers anyways

Capacitor Geometries

- Horizontal parallel plate
- Vertical parallel plate
- Combinations

“MOM” Capacitors

- Metal-Oxide-Metal capacitor. Free with modern CMOS.
- Use lateral flux ($\sim L_{\text{min}}$) and multiple metal layers to realize high capacitance values

MOM Capacitor Cross Section

- Use a wall of metal and vias to realize high density
- More layers – higher density
  - May want to chop off lower layers to reduce $C_{\text{bot}}$
- Reasonably good matching and accuracy
Distributed Effects

- Can model IC resistors as distributed RC circuits.
- Could use transmission line analysis to find equivalent 2-port parameters.
- Inductance negligible for small IC structures up to \( \sim 10\text{GHz} \).
  \[ R \gg \omega L \]

Effective Resistance

- High frequency resistance depends on \( W \), e.g.:
  - \( W=1\mu \) 10k\( \Omega \) resistor works fine at 1GHz
  - \( W=5\mu \) 10k\( \Omega \) resistor drops to 5k\( \Omega \) at 1 GHz
- May need distributed model for accurate freq response
Capacitor Q

- Current density drops as you go farther from contact edge...

Double Contact Structure

- If contact on both edges,
  - R drops 4X
  - Can be a good idea even if not hitting distributed effects
What About Inductors?

- Mostly not used in analog/mixed-signal design
  - Usually too big
  - More of a pain to model than R’s and C’s
  - But they do occasionally get used
- Example inductor app.: shunt peaking
  - Can boost bandwidth by up to 85%!
  - Q not that important (L in series with R)
  - But frequency response may not be flat

Spiral Inductors

- Used widely in RF circuits for small L (~1-10nH).
- Use top metal for Q and high self resonance frequencies.
  - Very good matching and accuracy – if you model them right