Comparator Gain-Bandwidth

Example:

- 4Gb/s link
- Minimum ΔV: 1mV
- Vdd = 1V

→ $A_v > \frac{1V}{1mV} = 1000$ in < 250ps!

Comparator

- Specs and issues:
  - Clock rate $f_c$
  - Offset
  - Resolution
  - Hysteresis
  - Input cap

- Power dissipation
- CM rejection
- Kickback noise
- ...

Flash Converter

- Fast: one clock cycle per conversion
- High complexity: $2^n - 1$ comparators
- High input capacitance

Operational Amplifier?

$\begin{align*}
  f_{zmax} &= \frac{f_c}{3A_v} \\
  f_c &= \frac{2A_v}{3L} \\
  &= \frac{1000}{3 \times 250 \text{ps}} = 1.33 \text{THz}
\end{align*}$
Cascaded Amplifier

- Simplified bandwidth analysis:
  - Open-circuit time constants
  - (Not most accurate, but leads to nearly the right answer for design optimization)

Power Consumption

Bandwidth/Gain Optimization

Regenerative Latch

CML Comparator (Latch)
Kickback cont'd