Offset

- To achieve zero offset, comparator devices must be perfectly matched to each other.

- How well-matched can the devices be made?
  - Not arbitrary – direct function of design choices.
Device Mismatch Categories

- **Die-to-die**
  - All devices on same chip (or wafer) have same characteristics

- **Within die (long-range)**
  - All devices within certain region have same characteristics

- **Local (short-range)**
  - Every device different, random
  - Usually most important source of mismatch

Sources of Local Variation

- **Deterministic sources:**
  - Local poly density
  - Sub-90nm: stress, litho interactions, ...

- **Random sources:**
  - Dopant fluctuations
  - Line-edge roughness
  - Oxide traps

- **Focus our modeling on random variations**
  - Deterministic handled with good layout practices
References

  - Mismatch model
  - Statistical data for 2.5µm CMOS

  - 0.18µm CMOS data

Mismatch Statistics

- Total mismatch set by composite of many single, independent events
  - Correlation distance << device dimensions
  - E.g., number of dopant atoms implanted into the channel

- Individual effects are small: linear superposition holds

- Mismatch is zero mean, Gaussian distribution
Parameter Mismatch Model

\[ \sigma^2(\Delta P) = \frac{A_p^2}{WL} + S_p^2 D_s^2 \]

- \( \sigma^2(\Delta P) \): standard deviation of P
- \( WL \): active gate area
- \( D_s \): distance between device centers
- \( A_p \): measured area proportionality constant
- \( S_p \): measured distance proportionality constant,
  \[ \equiv 0 \text{ for "good" layout} \]

V_T Mismatch

- Mismatch in \( V_T \) between two identical devices:
  \[ \sigma^2 (\Delta V_T) = \frac{A_{V_T,NMOS}^2}{WL} + S_{V_T}^2 D_s^2 \]

  2.5\( \mu \text{m} \) CMOS process:
  \( A_{V_T,NMOS} \equiv 30 \text{ mV} \mu\text{m} \)
  \( A_{V_T,PMOS} \equiv 35 \text{ mV} \mu\text{m} \)

- Often largest source of offset
Drain Bias, $V_{DS}$

Δ$V_T$ largely independent of $V_{DS}$

Back-Gate Bias, $V_{SB}$

- Mismatch can depend on $V_{SB}$
- Why?
Current Matching, $\Delta I_D/I_D$

Strong bias dependence (we knew that already)

Current Factor

$\beta = \mu C_{av} \frac{W}{L}$
Sources of $\beta$ Mismatch

- Mobility variations
  - E.g., due to dopant variations, random defects

- Oxide thickness variation
  - Usually very well-controlled

- Edge roughness

Edge Model

\[
\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{\text{ox}})}{C_{\text{ox}}^2} + \frac{\sigma^2(\mu_n)}{\mu_n^2}
\]

For: $\sigma^2(W) \propto \frac{1}{L}$ and $\sigma^2(L) \propto \frac{1}{W}$

Simplifies to:

\[
\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_1^2}{WL^2} + \frac{A_2^2}{W^2L} + \frac{A^2_{\text{ox}}}{WL} + \frac{A_3^2}{WL} + S^2_{\beta}D^2
\]
Orientation Effects

- Si and transistors are not (perfectly) isotropic
- \( \rightarrow \) keep direction of current flow same!

Distance Effect
Process Dependence

- $AV_t$ tends to scale with technology
- Proportional to $t_{ox}$
- Also depends on doping level

0.18 $\mu$m CMOS
“Golden Rule” of Layout for Matching

- Everything you can think of might matter
  - Even whether or not there is metal above the devices

- How to avoid systematic errors?


Common Centroid Layout

- Cancels linear gradients
- Required for moderate matching
Simulating Mismatch

- Brute force: Monte Carlo
  - HSPICE “throws the dice”...