Why Modeling?
- Analog circuits more sensitive to detailed transistor behavior
  - Precise currents, voltages, etc. matter
  - Digital circuits have much larger "margin of error"
- Models allow us to reason about circuits
  - Provide window into the physical device and process
  - "Experiments" with SPICE much easier to do

Square Law Model Assumptions
- Charge density determined only by vertical field
- Drift velocity set only by lateral field
- Neglect diffusion currents ("magic" \( V_{th} \))
- Constant mobility
- And many more...

Levels of Abstraction
- Best abstraction depends on questions you want to answer
- Digital functionality:
  - MOSFET is a switch
- Digital performance:
  - MOSFET is a current source and a switch
- Analog characteristics:
  - MOSFET described by BSIM with 100’s of parameters?
  - MOSFET described by measurement results?

A Real Transistor
- Ultra-thin Gate Dielectric
- Direct Tunneling Current
- Quantum Effects
- Pocket Implant
  - Reverse short-channel effect
  - Slower output resistance scaling with \( L \)
- Short Channel Effects
  - Velocity Saturation and Overshoot
  - Source-end Velocity Limit
- S/D Engineering
  - S/D resistances
  - S/D leakage
- Retrograde Doping
  - Body effect
  - Body effect
To Make Matters Worse…

- Run-to-run parameter variations:
  - E.g. implant doses, layer thickness, dimensions
  - Affect $V_{TH}$, $\mu$, $C_{ox}$, $R$...

- In SPICE use device “corners”: nominal / slow / fast parameters (tt, ss, ff)
  - E.g. fast: low $V_{TH}$, high $\mu$, high $C_{ox}$, low $R$
  - Combine with supply & temperature extremes
  - Pessimistic but numerically tractable
    - improves chances for working Silicon

Corner example: $V_{TH}$

- Corners just shift $V_{th}$
  - Probably not real
  - (PMOS doesn’t look real anyways)

- Variations probably bigger than reality too
  - Fab wants you to buy everything they make

Now What?

- Rely purely on simulator to tell us how devices behave?
  - Models not always based on real measurements
  - Model extraction is hard
  - Models inherently compromise accuracy for speed

- Need to know about important effects
  - So that know what to look for
  - Model might be wrong, or doesn’t automatically include some effects
    - E.g., gate leakage

$I_D$: Velocity Saturation

- Drift velocity initially increases linearly with field
- Eventually carriers hit a “speed limit”
- In the limit, $I_D \propto (V_{GS} - V_{th})$
**I_d: Vertical Field Mobility Reduction**

- Mobility actually depends on gate field
  - “Hard to run when there is wind blowing you sideways (into a wall)”

- More technical explanation:
  - E-field pushes carriers close to the surface
  - Enhanced scattering lowers mobility

\[
\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_T) + \theta_B V_{SB}}
\]

**I_d: Weak Inversion Current**

- Current set by diffusion – borrow BJT equation:

\[
I_{ds} = \frac{W}{L} I_{ds,0} \exp \left( \frac{V_{GS} - V_T}{\frac{V_{TH}}{n}} \right) \left( 1 - \frac{V_{DS}}{V_{TH}} \right)
\]

**I_d: Sub-Threshold Region**

- Current doesn’t really go to 0 at \( V_{GS} = V_{th} \)

- Lateral BJT:

**I_d: Operating in Weak Inversion**

- Usually considered “slow”:
  - “large” \( C_{ds} \) for “little” current drive (see later)

- But, weak (or moderate) inversion becoming more common:
  - Low power
  - Submicron L means “high speed” even in weak inversion

- Not well modeled, matching poor:
  - \( V_{th} \) mismatch amplified exponentially
  - Avoid in mirrors

**I_d: Weak Inversion Channel Potential**

- “Base” controlled through capacitive divider

\[\delta V_B = \frac{C_{ov}}{C_{ov} + C_{dp}} \delta V_d \]

- Non-ideality factor of channel control \( n > 1 \):

\[n = 1 + \frac{C_{dp}}{C_{ov}} = 1 + \frac{\epsilon_{ov} \epsilon_{dp}}{\epsilon_{ov} \epsilon_{dp}}\]

- \( n \) varies somewhat with bias – const. approx. usually OK

**I_d: Moderate Inversion**

- Moderate inversion: both drift and diffusion contribute to the current.

- Closed form equations for this region don’t really exist.
Output Resistance: CLM

- “Channel Length Modulation”
  - Depletion region varies with $V_{DS}$
  - Changes effective channel length

- If perturbation is small:

$$I \approx \frac{1}{L} \delta L(V_{ds}) \approx \frac{1}{L} \left(1 + \frac{\delta L(V_{ds})}{L}\right) I_{ds0} = (1 + \lambda V_{ds})$$

Output Resistance Mechanisms

- All effects active simultaneously
- CLM at relatively low fields
- DIBL dominates for high fields
- SCBE at very high fields

Output Resistance: DIBL

- “Drain Induced Barrier Lowering”

- Drain controls the channel too
  - Charge gets imaged – lowers effective $V_{th}$
  - Model with $V_{th} = V_{th0} - \eta V_{DS}$

Output Resistance: SCBE

- “Substrate Current Body Effect”
- At high electric fields, get “hot” electrons
  - Have enough energy to knock electrons off Si lattice (impact ionization)

- Extra $e^- - h^+$ pairs – extra (substrate) current
  - Models usually empirical

$$I_{SCE} = \frac{1}{B_i} \frac{B_i}{V_{th0}} \exp \left(\frac{B_i}{V_{DS} - V_{th0}}\right)$$

Comprehensive Model: BSIM

- **Berkeley Short-channel IGFET Model (BSIM)**
  - Industry standard model for modern devices
  - BSIM3v3 is model for this course

- Typically 40-100+ parameters
  - Advanced software and expertise needed even to perform extraction

Modeling: Now What?

- No “simple”, convenient hand model...
  - $r_i$ is key for gain, but really hard to model
  - Missing important regions such as moderate inversion

- Hand models really best to build intuition

- But for design (i.e., how to choose $W$, $L$, etc.):
  - Will learn how to use the simulator as a “calculator”