High Performance Signaling

Sources:
Dally, Poulton, “Digital Systems Engineering”,
Bakoglu, “Circuits, Interconnections and Packaging for VLSI”,
Addison-Wesley, 1990.

Limits of Electrical Signaling

Horowitz, Yang, Sidiropoulos,
“High-Speed Electrical Signaling: Overview and Limitations,”
IEEE Micro, 1/98
Multiplexed Transmitter

Data generation

Encoder

Predriver

Sync

Mux

Driver

Different on- and off-chip bandwidths
Transmitters have to drive low impedance

Multiplexer

UC Berkeley EE241
B. Nikolic
Tx Multiplexer

Pulse width limited

Overlapped signals

From Horowitz

Performance Limit

Eye closure vs. Bit width (HFO-4)
Demultiplexing Receiver

Demultiplexing Data
PLLs vs. DLLs

Voltage-controlled oscillator (VCO)

Clk

Phase detector

Ref clk

Vc

Filter

Voltage-controlled delay line (VCDL)

Clk

Phase detector

Ref clk

Vc

Filter

PLL and DLL Response

Response to a supply step

DLL peak

Phase error (degrees)

PLL peak

Time (ns)

0 500 1,000 1,500

0 -10 -20 -30 -40 -50

DLL

PLL f_{BW} 20 MHz

PLL f_{BW} 5 MHz
Delay Element and Interpolator

Phase Picking

Phase-picking data recovery
Clock waveforms are oversampling the data stream
Cable properties

Frequency response
12-meter and 6-meter RG-55U

Time domain response of a square pulse into 12m cable

Predistorted Pulse

Amplitude (V)

Time (ns)
4-PAM Data Eye

- Amplitude (V)
- Time (sec)

Power and Ground Distribution

(a) Finger-shaped network
(b) Network with multiple supply pins
Power Distribution

- Supply current is brought on chip at specific locations
  - on the edge for most chips which are peripherally bonded
  - distributed over the area of the chip for area bonded (C4, solder ball) chips
- Loads consume this current at different locations on the chip at different times
- There is often a large parasitic inductance associated with each bond-wire or solder-ball (0.1-10nH)

- Current is distributed from the bond pads to the loads on thin metal wires
  - 0.04Ω/ typical
- Load currents may be very high
  - average current may be as large as 20A for very hot chips (50W at 2.5V)
  - peak current may be 4-5x this amount (100A!)
- L di/dt of bond wire and IR drop across on-chip wires are often a major source of supply noise

From [Dally]

On-Chip Bypass Capacitors

- Much of the difference between peak and average current may be supplied by local, on-chip bypass capacitors
- Bypass capacitors are also critical in mitigating the effects of the supply bond-wire inductance