Delayed Precharge

(a) 

(b)
IBM’s 1GHz Processor

Domino Properties

- Logic evaluation propagates as falling dominoes
- Evaluation period determines the logic depth
- The nodes must be precharged during the precharge period (can limit the minimum size of PMOS)
- Inputs must be stable (or have only one rising transition) during the evaluation
- Gates are ratioless
- Restorer is ratioed
- All the gates are non-inverting
- Only one transition to be optimized
Multiple-Output Domino (MODL)

\[ F = F_1 F_2 \]

Common subexpressions

Hwang, Fisher, ISSCC’88

Lookahead Adder

Generate

Propagate
Lookahead Adder

4-bit group generate

4-bit group propagate

Compound Domino

Houston et al,
U.S. Pat. 5,015,882
May 1991.
Clock-Delayed Domino

Possible implementation of delay block

No need for inversion
Used in IBM’s 1GHz integer processor (ISSCC’98)
NTP Domino

Noise-tolerant precharge (NTP)

Yamada, ICCD’95

Output-Prediction Logic

Inverting logic:

Output-prediction logic:

McMurchie, et al, ICCD’2000
Output-Prediction Logic

NOR3:

Clocking:

McMurchie, et al, ICCD'2000

Output-Prediction Logic

NOR3 chain of 10:

Clock separation:
np-CMOS

Only $1 \rightarrow 0$ transitions allowed at inputs of PUN

Goncavles, De Man JSSC 6/83
Friedman, Liu, JSSC 4/84

np-CMOS

One-bit adder

$C_0 = AB + AC + BC$, $S = A \odot B \odot C$
NORA Logic

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NORA Logic

(a) \(\phi\)-module

(b) \(\bar{\phi}\)-module

Combinational logic  Latch

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NORA Logic

Fig. 7. Precharge racefree—precharge signal altered by the inputs:

\[ N1: \quad 1 \rightarrow 0 \left[ \phi = 1 \rightarrow \text{impossible} \right] \quad N1: \quad 0 \rightarrow 1 \left[ \phi = 0 \rightarrow \text{impossible} \right]. \]

\[ N2: \quad 0 \rightarrow 1 \left[ \phi = 0 \right] \quad N2: \quad 1 \rightarrow 0 \left[ \phi = 1 \right]. \]

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Fig. 8. Input variation racefree—precharge signal kept by the inputs.
NORA Logic

Fig. 9. Input variation racefree—sequence of dynamic blocks with pre-charge signals kept by the inputs:

$n$-type

\[
\begin{align*}
NX: 1 &\rightarrow 0 \\
\phi &= 1 \rightarrow \text{impossible}\* \\
NY: 0 &\rightarrow 1 \\
\phi &= 0 \\
\end{align*}
\]

$p$-type

\[
\begin{align*}
NX: 0 &\rightarrow 1 \\
\bar{\phi} &= 0 \rightarrow \text{impossible}\* \\
NY: 1 &\rightarrow 0 \\
\bar{\phi} &= 1 \\
\end{align*}
\]

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Fig. 10. Input variation racefree—even inversions between two $C^2$MOS latch stages:

"1" modification

\[
\begin{align*}
N1: 1 &\rightarrow 0 \\
\phi &= 1 \rightarrow \text{impossible}\* \\
N2, NX: 0 &\rightarrow 1 \\
\phi &= 0 \\
\end{align*}
\]

"0" modification

\[
\begin{align*}
N1: 0 &\rightarrow 1 \\
\phi &= 0 \rightarrow \text{impossible}\* \\
N2, NX: 1 &\rightarrow 0 \\
\bar{\phi} &= 1 \\
\end{align*}
\]

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Fig. 11. Precharge racefree—even inversions between the C^2MOS output stage and the last dynamic block.

Fig. 12. Input variation racefree—even inversions between the C^2MOS input stage and one dynamic block.

Zipper Logic

Lee, Szeto, Circuits and Devices 5/86
Zipper Logic

Type I:

Type II:

Clock and Data Precharged Logic

Domino

CDPD

Yuan, Svensson, Larson, Electronics Letters, 12/93
Clock and Data Precharged Logic

Logic chains

Differential (Dual Rail) Domino

Dynamic CVSL (Clock CVSL) - Heller et al, ISSCC'84
Dual-Rail Domino