Delayed Precharge
 Domino Properties

- Logic evaluation propagates as falling dominoes
- Evaluation period determines the logic depth
- The nodes must be precharged during the precharge period (can limit the minimum size of PMOS)
- Inputs must be stable (or have only one rising transition) during the evaluation
- Gates are ratioless
- Restorer is ratioed
- All the gates are non-inverting
- Only one transition to be optimized
Multiple-Output Domino (MODL)

F = F_1F_2

Common subexpressions

Hwang, Fisher, ISSCC’88

Lookahead Adder
Lookahead Adder

4-bit group generate

4-bit group propagate

Compound Domino

Houston et al,
U.S. Pat. 5,015,882
May 1991.
Clock-Delayed Domino

Possible implementation of delay block

No need for inversion
Used in IBM's 1GHz integer processor (ISSCC'98)
NTP Domino

Noise-tolerant precharge (NTP)

\[ \phi \]

(c) Yamada, ICCD'95

Output-Prediction Logic

Inverting logic:

\[ \text{gate1} \quad 1 \quad \text{gate2} \quad 0 \quad \text{gate3} \quad 1 \quad \text{gate4} \quad 0 \]

Output-prediction logic:

\[ \text{gate1} \quad 1 \quad \text{gate2} \quad 1 \quad \text{gate3} \quad 1 \quad \text{gate4} \quad 1 \]

McMurchie, et al, ICCD'2000
Output-Prediction Logic

NOR3:

Clocking:

NOR3 chain of 10:

Clock separation:

McMurchie, et al, ICCD'2000
np-CMOS

Only 1→0 transitions allowed at inputs of PUN
Goncavles, De Man JSSC 6/83
Friedman, Liu, JSSC 4/84

np-CMOS

One-bit adder

\[ C_0 = AB + AC_1 + BC_1 \]
\[ S = A \oplus B \oplus C \]
NORA Logic

UC Berkeley EE 241
B. Nikolić

NORA Logic

UC Berkeley EE 241
B. Nikolić
Fig. 7. Precharge racefree—precharge signal altered by the inputs:

\[ \begin{align*}
N1: & \quad 1 \rightarrow 0 \quad \phi = 1 \rightarrow \text{impossible}^* \\
N2: & \quad 0 \rightarrow 1 \quad \phi = 0 \\
N1: & \quad 0 \rightarrow 1 \quad \phi = 0 \rightarrow \text{impossible}^* \\
N2: & \quad 1 \rightarrow 0 \quad \phi = 1
\end{align*} \]

Fig. 8. Input variation racefree—precharge signal kept by the inputs.
NORA Logic

Fig. 9. Input variation racefree—sequence of dynamic blocks with pre-charge signals kept by the inputs:

<table>
<thead>
<tr>
<th>n-type</th>
<th>p-type</th>
</tr>
</thead>
<tbody>
<tr>
<td>$NX: 1 \to 0$</td>
<td>$NX: 0 \to 1$</td>
</tr>
<tr>
<td>$\phi = 1 \to$ impossible*</td>
<td>$\bar{\phi} = 1 \to$ impossible*</td>
</tr>
<tr>
<td>$NY: 0 \to 1$</td>
<td>$NY: 1 \to 0$</td>
</tr>
<tr>
<td>$\phi = 0$</td>
<td>$\bar{\phi} = 1$</td>
</tr>
</tbody>
</table>

NORA Logic

Fig. 10. Input variation racefree—even inversions between two $\text{C}^2\text{MOS}$ latch stages:

"1" modification

| $N1: 1 \to 0$ | $N1: 0 \to 1$ |
| $\phi = 1 \to$ impossible* | $\bar{\phi} = 0 \to$ impossible* |
| $N2, NX: 0 \to 1$ | $N2, NX: 1 \to 0$ |
| $\phi = 0$ | $\bar{\phi} = 1$ |

"0" modification
NORA Logic

Fig. 11. Precharge racefree—even inversions between the C$^2$MOS output stage and the last dynamic block.

Fig. 12. Input variation racefree—even inversions between the C$^3$MOS input stage and one dynamic block.

Zipper Logic

Lee, Szeto, Circuits and Devices 5/86
Zipper Logic

Type I:

Type II:

Clock and Data Precharged Logic

Domino

CDPD

Yuan, Svensson, Larson, Electronics Letters, 12/93
Clock and Data Precharged Logic

Logic chains

Differential (Dual Rail) Domino

Dynamic CVSL (Clock CVSL) - Heller et al, ISSCC’84
Dual-Rail Domino