Low Power, Low Energy Circuit Design

Architectures, Circuits and Technology
Literature

- Chapter 4, Low-Voltage Technologies, by Kuroda and Sakurai
- Chapter 3, Techniques for Leakage Power Reduction, by De, et al.
- Proceedings of the IEEE, Special Issue on Low Power, April 1995.

Power vs. Energy

- Power in high performance systems
  » Peak power - power delivery, removal
- Energy in portable systems
  » Battery life
- Constant throughput vs. burst-mode computation
- Active vs. standby consumption
Power in CMOS

\[ P \sim \alpha \cdot (C_L \cdot V_{\text{swing}} + \overline{I_{\text{SC}}} \cdot \Delta t_{\text{SC}}) \cdot V_{\text{DD}} \cdot f + (I_{\text{DC}} + I_{\text{Leak}}) V_{\text{DD}} \]

- \( \alpha \) - switching probability
- \( C_L \) – load capacitance
- \( V_{\text{swing}} \) – voltage swing
- \( f \) - frequency

Dominant: \( P \sim \alpha \cdot C_L \cdot V_{\text{swing}} \cdot V_{\text{DD}} \cdot f \)

Trends in Power Dissipation

(a) Power dissipation vs. year.

(b) Power density vs. scaling factor.

From Kuroda
Processor Power

Lead processor power increases every generation
Compactions provide higher performance at lower power

Power will be a problem

Power delivery and dissipation will be prohibitive

UC Berkeley EE241
B. Nikolić
Portability

Required Portable Functions

- Radio transceiver
- Modem
- Voice I/O
- Pen Input
- Text/Graphics Processing
- Text/Graphics display
- Video decompression
- Full-motion video display

How to get 8 hours of operation ???

Battery Life

(from Jon Eager, Gates Inc., S. Watanabe, Sony Inc.)
**Shannon Beats Moore’s Law**

- **Algorithmic Complexity (Shannon’s Law)**
- **Processor Performance (~Moore’s Law)**
- **Battery Capacity**

**Where Does Power Go in CMOS?**

- **Dynamic Power Consumption**
  Charging and Discharging Capacitors

- **Leakage**
  Leaking transistors and diodes

- **Short Circuit Currents**
  Short Circuit Path between Supply Rails during Switching

- **Review basics from Rabaey’s Digital ICs**
Dynamic Power Consumption

\[ E_{0 \rightarrow 1} = \int_0^T P(t) \, dt = V_{dd} \int_0^T i_{\text{supply}}(t) \, dt = V_{dd} \int_0^T i_{\text{supply}} \, dt = \frac{1}{2} CL V_{dd}^2 \]

\[ E_{\text{cap}} = \int_0^T P_{\text{cap}}(t) \, dt = V_{out} \int_0^T i_{\text{cap}}(t) \, dt = V_{out} \int_0^T i_{\text{cap}} \, dt = \frac{1}{2} CL V_{out}^2 \]

Circuits with Reduced Swing

\[ E_{0 \rightarrow 1} = CL \cdot V_{dd} \cdot (V_{dd} - V_t) \]

- Can exploit reduced swing to lower power
  (e.g., reduced bit-line swing in memory)
Dynamic Power Consumption - Revisited

Power = Energy/transition * transition rate
= \( C_L \cdot V_{dd}^2 \cdot f_{0\rightarrow1} \)
= \( C_L \cdot V_{dd}^2 \cdot P_{0\rightarrow1} \cdot f \)
= \( C_{EFF} \cdot V_{dd}^2 \cdot f \)

Power Dissipation is Data Dependent
Function of Switching Activity

\( C_{EFF} \) = Effective Capacitance = \( C_L \cdot P_{0\rightarrow1} \)

Node Transition Activity and Power

● Consider switching a CMOS gate for \( N \) clock cycles

\( E_N = C_L \cdot V_{dd}^2 \cdot n(N) \)

\( E_N \): the energy consumed for \( N \) clock cycles
\( n(N) \): the number of 0->1 transition in \( N \) clock cycles

\( P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \cdot f_{clk} = \left( \lim_{N \to \infty} \frac{n(N)}{N} \right) \cdot C_L \cdot V_{dd}^2 \cdot f_{clk} \)

\( \alpha_{0\rightarrow1} = \lim_{N \to \infty} \frac{n(N)}{N} \)

\( P_{avg} = \alpha_{0\rightarrow1} \cdot C_L \cdot V_{dd}^2 \cdot f_{clk} \)
Type of Logic Function: NOR

Example: Static 2 Input NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table of a 2 input NOR gate

Assume:
\[ p(A=1) = 1/2 \]
\[ p(B=1) = 1/2 \]

Then:
\[ p(\text{Out}=1) = 1/4 \]
\[ p(0 \rightarrow 1) = p(\text{Out}=0) \cdot p(\text{Out}=1) \]
\[ = 3/4 \times 1/4 = 3/16 \]

\[ \alpha_{0 \rightarrow 1} = 3/16 \]

Type of Logic Function: XOR

Example: Static 2 Input XOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table of a 2 input XOR gate

Assume:
\[ p(A=1) = 1/2 \]
\[ p(B=1) = 1/2 \]

Then:
\[ p(\text{Out}=1) = 1/2 \]
\[ p(0 \rightarrow 1) = p(\text{Out}=0) \cdot p(\text{Out}=1) \]
\[ = 1/2 \times 1/2 = 1/4 \]

\[ \alpha_{0 \rightarrow 1} = 1/4 \]
Transition Probabilities

$P_{0\rightarrow 1}(\text{NOR, NAND}) = \frac{(2^N - 1)}{2^{2N}}$  
$P_{0\rightarrow 1}(\text{XOR}) = 1/4$

Transition Probabilities for Basic Gates

<table>
<thead>
<tr>
<th>Gate</th>
<th>$P_{0\rightarrow 1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND</td>
<td>$(1 - P_A P_B) P_A P_B$</td>
</tr>
<tr>
<td>OR</td>
<td>$(1 - P_A)(1 - P_B)(1 - P_A)(1 - P_B)$</td>
</tr>
<tr>
<td>EXOR</td>
<td>$(1 - (P_A + P_B - 2P_A P_B))(P_A + P_B - 2P_A P_B)$</td>
</tr>
</tbody>
</table>

Switching Activity for Static CMOS

$P_{0\rightarrow 1} = P_0 P_1$
**Transition Probability of 2-input NOR Gate**

\[ p_1 = (1-p_a)(1-p_b) \]
\[ p_{0->1} = p_a p_b = (1-(1-p_a)(1-p_b))(1-p_a)(1-p_b) \]

- \( p_{0->1} \) is a strong function of signal statistics

**How about Dynamic Circuits?**

Power is only dissipated when Out = 0!

\[ C_{EFF} = P(Out=0)C_L \]
2-input NAND Gate

Example: Dynamic 2 Input NOR Gate

Assume:
\[ P(A=1) = \frac{1}{2} \]
\[ P(B=1) = \frac{1}{2} \]

Then:
\[ P(\text{Out}=0) = \frac{3}{4} \]

\[ C_{\text{EFF}} = \frac{3}{4} \times C_L \]

Switching Activity Is Always Higher in Dynamic Circuits

Type of Logic Style:
Static vs. Dynamic

Power is only dissipated when Out=0!

\[ \alpha_{0 \rightarrow 1} = \frac{3}{16} \]

\[ \alpha_{0} \rightarrow 1 = \frac{N_0}{N} = \frac{3}{4} \]
Transition Probabilities for Dynamic Gates

<table>
<thead>
<tr>
<th>Operation</th>
<th>$P_{0\to1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND</td>
<td>$(1-P_A P_B)$</td>
</tr>
<tr>
<td>OR</td>
<td>$(1-P_A)(1-P_B)$</td>
</tr>
<tr>
<td>EXOR</td>
<td>$(1 - (P_A + P_B - 2P_A P_B))$</td>
</tr>
</tbody>
</table>

Switching Activity for Precharged Dynamic Gates

$$P_{0\to1} = P_0$$

Another Logic Style: Dynamic DCVSL

Guaranteed transition for every operation!

$$\alpha_{0\to1} = 1$$
Reconvergent Fanout

(a) Logic circuit without reconvergent fanout

\[ P_{0 \rightarrow 1} = (1 - p_a p_b) p_a p_b = 3/16 \]

(b) Logic circuit with reconvergent fanout

\[ P_Z = P(C=1|B=1) \cdot P(B=1) \]

\[ P_{0 \rightarrow 1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations!
- CAD tools required for such analysis
Glitching in Static CMOS

also called: dynamic hazards

\[ \begin{array}{c}
A \\
B \\
X \\
C \\
Z \\
\end{array} \]

<table>
<thead>
<tr>
<th>ABC</th>
<th>101</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td></td>
</tr>
</tbody>
</table>

Observe: No glitching in dynamic circuits

Example 1: Chain of NOR Gates

![Diagram of chain of NOR gates and voltages over time](image)
Example 2: Adder Circuit

<table>
<thead>
<tr>
<th>Sum Output Voltage, Volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cin</td>
</tr>
<tr>
<td>0.0</td>
</tr>
<tr>
<td>2.0</td>
</tr>
<tr>
<td>4.0</td>
</tr>
<tr>
<td>Time, ns</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

How to Cope with Glitching?

Equalize Lengths of Timing Paths Through Design
Example: Carry Ripple versus Carry Lookahead

Ripple

Lookahead

Short Circuit Currents

UC Berkeley EE241 B. Nikolić
**Short Circuit Currents - Unloaded**

\[
I_{m.cn} = 2 \cdot \frac{2}{T_{cl}} \int_{t_1}^{t_2} \frac{\beta}{2} (V_{DD} - 2V_{th})^3 \cdot \frac{2}{T_{cl}} dt
\]

\[
I_{m.cn} = \frac{\beta}{12} \frac{V_{DD}}{(V_{DD} - 2V_{th})^3} \cdot \frac{2}{T_{cl}}
\]

\[
P_{sc} = V_{DD} \cdot I_{m.cn} = \frac{\beta}{12} (V_{DD} - 2V_{th})^3 \cdot \tau \cdot \eta_d
\]

**Impact of rise/fall times on short-circuit currents**

Large capacitive load

Small capacitive load
How to keep Short-Circuit Currents Low?

Keep Input and Output Rise/Fall Times the Same. 
(< 20% of Total Consumption)

Static Power Consumption

\[ P_{\text{stat}} = P_{(I_{\text{n}}=1)} \cdot V_{dd} \cdot I_{\text{stat}} \]

- Dominates over dynamic consumption
- Not a function of switching frequency
Leakage

Sub-Threshhold Current Dominant Factor

Sub-Threshold in MOS

Lower Bound on Threshold to Prevent Leakage
Subthreshold Leakage Component

- Leakage control is critical for low-voltage operation

Projected Leakage

0.1μm, 15mm die, 0.7V

- Leakage
- Active