## Announcements

- Project reports/posters
  - Title/names
  - Motivation
  - Problem statement
  - Possible solutions from literature
  - Proposed comparison/solution
  - Conditions/assumptions
  - Analysis
  - Outline of proposed design work
  - Conclusion
  - References
Literature

- Chapter 4, Low-Voltage Technologies, by Kuroda and Sakurai
- Chapter 3, Techniques for Leakage Power Reduction, by De, et al.
- Materials by T. Sakurai, ISSCC Workshop, 2001
Leakage Components

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection

Drain-induced barrier lowering (DIBL)
- Voltage at the drain lowers the source potential barrier
- Lowers VT, no change on S

Gate-induced drain leakage (GIDL)
- High field between gate and drain increases injection of carriers into substrate -> leakage
  (band-to-band leakage)
DIBL, GIDL, Weak Inversion

Stack Effect

NAND gate:

Reduction:

<table>
<thead>
<tr>
<th>A &amp; B = 0</th>
<th>( V_{in} - V_T )</th>
</tr>
</thead>
<tbody>
<tr>
<td>High ( V_T )</td>
<td>Low ( V_T )</td>
</tr>
<tr>
<td>2 NMOS</td>
<td>10.7X</td>
</tr>
<tr>
<td>3 NMOS</td>
<td>21.1X</td>
</tr>
<tr>
<td>4 NMOS</td>
<td>31.5X</td>
</tr>
<tr>
<td>2 PMOS</td>
<td>8.6X</td>
</tr>
<tr>
<td>3 PMOS</td>
<td>16.1X</td>
</tr>
<tr>
<td>4 PMOS</td>
<td>23.1X</td>
</tr>
</tbody>
</table>
Gate Leakage

Trends

Gate voltage (V) vs. Gate current density (A/cm²)

Gate Leakage


Working with Leakage

- Multi VTH, multi VDD design
  - Gate level/Synthesis approaches
  - “Random modulation”
  - Transistor-level multi-VTH design
- Standby/runtime leakage control
  - MTCMOS/ power-down
  - Substrate bias (VTCMOS)
    - Self-substrate bias (SSB)
    - Self-adjusting threshold voltage (SAT)
    - Standby power reduction (SPR)
    - SAT+SPR
VDD and VTH Control

Spatial control: multiple VDDs, VTHs
Temporal control: variable VDDs, VTHs

<table>
<thead>
<tr>
<th></th>
<th>Active</th>
<th>Stand-by</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiple $V_{TH}$</td>
<td>Multi-$V_{TH}$</td>
<td>MTMOS</td>
</tr>
<tr>
<td>Variable $V_{TH}$</td>
<td>$V_{TH}$ hopping</td>
<td>VTMCOS</td>
</tr>
<tr>
<td>Multiple $V_{DD}$</td>
<td>Multi-$V_{DD}$</td>
<td>Boosted gate MOS</td>
</tr>
<tr>
<td>Variable $V_{DD}$</td>
<td>DVS</td>
<td></td>
</tr>
</tbody>
</table>

Using Multiple Thresholds

- Cell-by-cell $V_T$ assignment (not block level)
- Allows us to minimize leakage
- Achieves all-low-$V$ performance
Dual VT Domino

Multiple Supplies

Conventional Design

CVS Structure

Lower $V_{DD}$ portion is shaded

"Clustered voltage scaling"
Multiple Supplies

CVS

Layout:

Level Converting Flip-Flop

UC Berkeley EE241

B. Nikolić
Techniques for Burst Mode Computation

Multiple $V_T$ technology
(Disable high $V_T$ devices during idle periods)
e.g. [Sakata93](Symposium on VLSI circuits)
[Mutoh93] (International ASIC conference)

- High $V_T$ transistor sizing issues
- Preserving state requires extra transistors

MTCMOS

Latch Design in MTCMOS

[Mutoh95]

Boosted-Gate MOS (BGMOS)

CMOS circuits
- low $V_{TH}$
- ultra thin $T_{OX}$

Virtual $V_{SS}$

Leak cut-off Switch (LS)
- high $V_{TH}$
- thick $T_{OX}$

Eliminates tunneling
### VTCMOS Variants

<table>
<thead>
<tr>
<th>SA</th>
<th>SPR (steady state selection)</th>
<th>SPR - SA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{THA}$ (active) (&lt;br&gt; standby)</td>
<td>$V_{THA} = 0.3$ V</td>
<td>$V_{THA} = 0.3$ V</td>
</tr>
<tr>
<td>$V_{THA}$ (active) (&lt;br&gt; standby)</td>
<td>$V_{THA} = 0.5$ V</td>
<td>$V_{THA} = 1.2$ V</td>
</tr>
<tr>
<td>$V_{TH}$ (standby)</td>
<td>$V_{TH} = 2.0$ V</td>
<td>$V_{TH} = 0.3$ V</td>
</tr>
</tbody>
</table>

**Normalized Delay vs $V_{DD}$ & $V_{TH}$**

![Normalized Delay vs $V_{DD}$ & $V_{TH}$](image)

**VDD** = 1.0 V

$\Delta V_{TH} = \pm 0.15 V, \pm 0.05 V$

Sakurai, Kuroda

UC Berkeley EE241

B. Nikolić
Self-Adjusting Threshold-Voltage Scheme (SATS)

low $V_{th}$ → large leakage → SSB ON → deep $V_{BB}$ → high $V_{th}$

high $V_{th}$ → little leakage → SSB OFF → shallow $V_{BB}$ → low $V_{th}$

- control $V_{th}$ to adjust leakage current
- compensate $V_{th}$ fluctuation

SATS Experimental Results

Vth controllability $\pm 0.05$V
Substrate Bias Effect

\[ V_{TH} = V_{T0} - \gamma \sqrt{2\phi_F - V_{BS}} = V_{T0} - \gamma V_{BS} \]

Techniques for Burst Mode Computation

- Needs large body factors - large well capacitances
- Triple well process needed

from [Seta95] (ISSCC 1995)
Standby Power Reduction (SPR)

SPR Waveforms (SPICE)
VT (Variable Threshold-Voltage) CMOS

ISSCC'96 pp.166-167

VDD+3.3V @standby
VDD+0.5V @active
- 0.55V @standby
- 0.15V @active
Vth,n: 0.15V @active
0.55V @standby
- 0.5V @active
- 3.3V @standby

VT

VT-CMOS:
Dynamic Vth control for low power through backgate bias
example:
(SATS) or (SPR) or (SATS + SPR)

Kuroda, JSSC 11/96

Substrate Bias in VT

power-on
active mode
power line
standby mode

Vactive = -0.3V
Vactive = 0.5V
Vactive = 0.7V
Vstandby = 3.3V

SSB-50MHz (100μA)
SSB 5MHz (12mA)
SCI-on (30mA)
SCI-off
SSB-50MHz (100μA)

Kuroda, JSSC 11/96
## VTCMOS vs. MTCMOS

<table>
<thead>
<tr>
<th>Principle</th>
<th>VTCMOS</th>
<th>MTCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Threshold control with sub-bias</strong></td>
<td></td>
<td>On-off control of internal VDD/VSS</td>
</tr>
<tr>
<td><strong>Merit/ Demerit</strong></td>
<td>○ Low leakage in standby - Needs circuit development + Compensate (\Delta V)th fluctuation + IDDQ test + No serial MOSFET ○ Conventional design tools + Reuse of existing design - Triple well is desirable</td>
<td>○ Low leakage in standby + Conceptually easier - Compensate (\Delta V)th fluctuation - IDDQ test - Large serial MOSFET slower, larger, lower yield... ○ Conventional design tools - Special (\overline{F/F})'s + Conventional well structure</td>
</tr>
</tbody>
</table>