Overview

- Synchronous Systems
  » Timing methodologies
  » Latching elements
  » Clock distribution
  » Clock generation
- Asynchronous Systems
References

- Chapter 11 – Clocked storage elements, by H. Partovi
- Unger/Tan IEEE Trans. Comp. 10/86
- Harris/Horowitz JSSC 11/97
- Stojanović/Oklobdžija JSSC 4/99

Latch versus Flip-Flop

- Latch stores data when clock is low
- Flip-Flop stores data when clock rises
Latch Parameters

```
Clk
D Q

Q
T_{Clk-Q}
```

```
Clk
D Q

Q
T_{Clk-Q}
```

Delays can be different for rising and falling data transitions

Unger and Tan
Trans. on Comp.
10/86

Flip-Flop Parameters

```
Clk
D Q

Q
T_{Clk-Q}
```

```
Clk
D Q

Q
T_{Clk-Q}
```

Delays can be different for rising and falling data transitions

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Clock Nonidealities

- **Clock skew**
  » Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$

- **Clock jitter**
  » Temporal variations in consecutive edges of the clock signal; modulation + random noise
  » Cycle-to-cycle (short-term) $t_{JS}$
  » Long term $t_{JL}$

- **Variation of the pulse width**
  » for level sensitive clocking
Clock Skew and Jitter

Both skew and jitter affect the effective cycle time.
Only skew affects the race margin.

Clock Skew

Earliest occurrence of Clk edge:
Nominal - \( T_{sk}/2 \)

Latest occurrence of Clk edge:
Nominal + \( T_{sk}/2 \)

Max Clk skew:
\( T_{sk} \)
Positive and Negative Skew

(a) Positive skew

(b) Negative skew

Constraints on Skew

(a) Race between clock and data.

(b) Data should be stable before clock pulse is applied.
Longest Logic Path in Edge-Triggered Systems

If launching edge is late and receiving edge is early, the data will not be too late if:

\[ P - T_{sk} + T_{JS} - T_{SU} \geq T_{clk-QM} + T_{LM} \]

Minimum cycle time is determined by the maximum delays through the logic

\[ P \geq T_{clk-QM} + T_{LM} + T_{SU} + T_{sk} + T_{JS} \]

‘Double-sided’ definitions of setup and jitter

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Shortest Path

Earliest point of launching

Clk

\[ T_{Clk-Q} \]

\[ T_{Lm} \]

Clk

\[ T_H \]

Nominal clock edge

Data must not arrive before this time

Clock Constraints in Edge-Triggered Systems

If launching edge is early and receiving edge is late:

\[-T_{clk-Qm} + T_{Lm} \geq T_{sk} + T_H\]

Minimum logic delay

\[ T_{Lm} \geq T_{sk} + T_H - T_{clk-Qm} \]
Clock Constraints in Edge-Triggered Systems

Flip-Flop – Based Timing
Flip-Flops and Dynamic Logic

Flip-flops are used only with static logic

Latch timing

When data arrives to transparent latch
Latch is a ‘soft’ barrier

When data arrives to closed latch
Data has to be ‘re-launched’
### Single-Phase Clock with Latches

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![Single-Phase Clock with Latches Diagram]

### Preventing Late Arrivals

Data must arrive

![Preventing Late Arrivals Diagram]
Preventing Late Arrivals

\[
P \geq \max \left\{ \frac{T_{skl} + T_{skt} + T_{SU} + T_{clk-QM} - PW}{T_{D-QM}} \right\} + T_{LM}
\]

Or:

\[
P \geq T_{clk-QM} + T_{LM} + T_{SU} + T_{skl} + T_{skt} - PW
\]

\[
P \geq T_{D-QM} + T_{LM}
\]

Preventing Premature Arrivals

Two cases, reduce to one:

\[
T_{Lm} \geq T_{skl} + T_{skt} + T_{H} + PW - T_{Clk-Qm}
\]
Single-Latch Timing

Bounds on logic delay:

\[ P \geq \max \left\{ T_{skl} + T_{skt} + T_{SU} + T_{clk - QM} - PW, T_{D - QM} \right\} + T_{LM} \]

\[ T_{Lm} \geq T_{skl} + T_{skt} + T_{H} + PW - T_{Clk - Qm} \]

Either balance logic delays or make PW short

Latch-Based Design

L1 latch is transparent when \( \phi = 0 \)

L2 latch is transparent when \( \phi = 1 \)
Latch-Based Timing

Can tolerate skew!

Latch-Based Timing

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Can tolerate skew!

Latch-Based Timing

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Latch-Based Timing

- Longest path
  \[ P \geq 2T_{D-QM} + T_{LHM} + T_{LLM} \]

- Short paths
  \[ T_{CLLm} \geq T_{SK} + T_H - T_{Clk-Qm} \]
  \[ T_{CLHm} \geq T_{SK} + T_H - T_{Clk-Qm} \]