EE241 - Spring 2001
Advanced Digital Integrated Circuits

Lecture 23
Clock Distribution and Generation

Reading

- Chapter 13, Clock Distribution by Bailey
- Chapter 12, PLLs and DLLs by Maneatis
Clock Uncertainty

- Clock skew (spatial uncertainty)
  - Systematic
  - Random
- Clock jitter (temporal uncertainty)
  - Short term: cycle-to-cycle changes

Clock Distribution

- Tree
  Common, e.g. IBM S/390
- Clock grid
- DEC Alpha
- Length-matched Serpentine
- Intel P6
Final Stage: Tree vs. Grid

RC-matched Tree

Grid

Predriver

Binary tree

H - tree

X - tree

Arbitrary matched tree


B. Nikolić
Clock Distribution

**H-Tree Network**

Observe: Only Relative Skew is Important

Example: PowerPC 603
Gerosa, JSSC 12/94

Clock Network with Distributed Buffering

Reduces absolute delay, and makes Power-Down easier
Sensitive to variations in Buffer Delay
Example IBM S/390

Clock Tree Delays

Webb, JSSC 11/97

Restle, VLSI'98
IR Emission Images

- Central buffer
- Sector buffers
- Clock repeaters
- Local clocks

Sanda, ISSCC'99

Example: DEC Alpha 21164
Clock Skew in Alpha Processor

DEC Alpha Evolution

Clock driver placements

Gronowski, JSSC 5/98
Clock Skews

Hybrid Grid

DEC Alpha 21264
Bailey JSSC 11/98
Alpha 21264

Alpha 21264 Grids

<table>
<thead>
<tr>
<th>Major Clock</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCLK</td>
<td>I/O interface unit</td>
</tr>
<tr>
<td>ECLK</td>
<td>Integer issue and execution units</td>
</tr>
<tr>
<td>FCLK</td>
<td>Floating-point issue and execution units</td>
</tr>
<tr>
<td>JCLK</td>
<td>Instruction fetch and branch prediction unit</td>
</tr>
<tr>
<td>MULK</td>
<td>Load/store unit</td>
</tr>
<tr>
<td>PLLK</td>
<td>pad ring</td>
</tr>
</tbody>
</table>
Data-Dependent Gate Loading

<table>
<thead>
<tr>
<th>Case</th>
<th>Gate Capacitance Spectrum</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.3 Case 1</td>
</tr>
<tr>
<td>2</td>
<td>1.1 Case 2</td>
</tr>
<tr>
<td>3</td>
<td>1.0 Case 3</td>
</tr>
<tr>
<td>4</td>
<td>.80 Case 4</td>
</tr>
<tr>
<td>5</td>
<td>.42 Case 5</td>
</tr>
<tr>
<td>6</td>
<td>.31 Case 6</td>
</tr>
<tr>
<td>7</td>
<td>.13 Case 7</td>
</tr>
</tbody>
</table>

Multi-GHz Clock Networks

Phillip Restle, IBM Research
IEEE SSCTC Workshop on Design for Multi-GigaHertz Processors,
San Francisco, Feb. 7, 2000

Clock Generation

Delay-Locked Loop (Delay Line Based)

\[ f_{\text{REF}} \rightarrow \text{Phase Det} \rightarrow \text{Charge Pump} \rightarrow \text{DL} \rightarrow f_o \]

Phase-Locked Loop (VCO-Based)

\[ f_{\text{REF}} \rightarrow \text{PD} \rightarrow \text{CP} \rightarrow \text{Filter} \rightarrow \text{VCO} \rightarrow f_o \]

Phase-Locked Loop Based Clock Generator

Acts also as Clock Multiplier
Loop Components

- **Phase Comparator**
  » Produces UP/DN pulses corresponding to phase difference
- **Charge Pump**
  » Sources/sinks current for duration of UP/DN pulses
- **Loop Filter**
  » Integrates current to produce control voltage
- **Voltage-Controlled Delay Line**
  » Changes delay proportionally to voltage
- **Voltage-Controlled Oscillator**
  » Generates frequency proportional to control voltage

DLL Locking


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PLL Jitter

Two clock spines, two DLLs, and a PD that controls them

Clock Deskewing

Two clock spines, two DLLs, and a PD that controls them

Geannopoulos, ISSCC'98
Clock Ring

Clocks routed in parallel, opposite directions
LCG aligns to the middle

Synchronous Distributed Oscillators

Mizuno, ISSCC'98
Distributed PLLs

Gutnik, ISSCC'2000

Intel Itanium™

Global Clock Distribution

Rusu, ISSCC'2000

- Balanced H-tree routed in M5 and M6
- Lateral shielding
- Distributes both main and reference clock
- Optimized to account for inductive effects
Intel Itanium™

Regional Clock Distribution

- Distributed array of deskew buffers to reduce process related skew
  - 8 deskew clusters each holding up to 4 buffers
- Regional clock grids driven by modular Regional Clock Drivers
  - M4-M5 grid tailored for the clock load density of the underlying block
  - Full support for scan and clock gating

**Legend**
- DSK = Cluster of 4 deskew buffers
- CDC = Central Deskew Controller

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