CVSL Properties

- Static
- No static power, except DSL leakage
- Process and supply tolerance is an issue with DSL
Pass-Transistor Logic Styles

- Static Pass-Transistor Logic
  - Transmission gates
  - Complementary PTL (CPL)
  - Dual (DPL)
  - Reduced DPL (DVL)
  - Swing restoration techniques – SRPL, SAPL, DCVSPG

Pass-Transistor Logic

- N transistors
- No static consumption
- Transistor implementation using NMOS
NMOS-only switch

\[ V_B \text{ does not pull up to } 2.5V, \text{ but } 2.5 - V_{TN} \]

Threshold voltage loss causes static power consumption

NMOS-Only Switch

\[ V_{DD}, V_{IN}, V_{OUT}, 0.5 \mu m/0.25 \mu m, 1.5 \mu m/0.25 \mu m \]
Pass-Transistor Logic Families

<table>
<thead>
<tr>
<th>Logic Load</th>
<th>NMOS Logic</th>
<th>Pass-Transistor Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS Cross-Couple</td>
<td>CVSL (IBM, 1984)</td>
<td>DCVSPG (IBM, 1993)</td>
</tr>
<tr>
<td>CMOS Inverter</td>
<td>DSL (Philips, 1985)</td>
<td>CPL (Hitachi, 1990)</td>
</tr>
<tr>
<td>None</td>
<td>DPL (Hitachi, 1993)</td>
<td>SRPL (Toshiba, 1994)</td>
</tr>
<tr>
<td>CMOS Latch</td>
<td></td>
<td>SAPL (Toshiba, 1994)</td>
</tr>
<tr>
<td>Sense-Amplifier</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Pass-Transistor Logic Families

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Complementary Pass-Transistor Logic (CPL)

- Complementary functions
- Reduced number of logic levels
- Much less transistors than CMOS
- Fast – reduced load
- Complementary inputs – complementary outputs
- $V_T$ drop – several solutions

CPL

Yano et al, CICC’89, JSSC 4/90
Complementary Pass-Transistor Logic (CPL)

- Fast
- $V_T$ drop
- Efficient implementation of arithmetic

XOR

Sum
CPL

Yano – CICC’89: 0.5µm CMOS with dual thresholds

WATCH OUT FOR LEAKAGE CURRENTS

Karnaugh Maps

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CPL vs. CMOS

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>CPL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor Count</td>
<td>40</td>
<td>28</td>
</tr>
<tr>
<td>Area</td>
<td>4730μm²</td>
<td>4218 μm²</td>
</tr>
<tr>
<td>Delay (4V)</td>
<td>0.63ns</td>
<td>0.26ns</td>
</tr>
<tr>
<td>Power (100MHz)</td>
<td>1.2mW</td>
<td>0.86mW</td>
</tr>
</tbody>
</table>

Skewing Output Inverter

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CPL vs. CMOS

Differential vs. Single-Ended

<table>
<thead>
<tr>
<th>Single-Ended Pass Transistor Logic</th>
<th>CPL</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLA Circuit</td>
<td></td>
</tr>
<tr>
<td>Transistor Count</td>
<td>82</td>
</tr>
<tr>
<td>Delay (C0→C0)</td>
<td>0.25ns</td>
</tr>
</tbody>
</table>
CPL Performance

- Implemented 16 x 16bit multiplier
- 3.8ns (@ 300K) in 0.5µm CMOS
- Wallace tree + CLA in final adder

CPL vs. Supply Voltage

![Graphs showing CPL vs. Supply Voltage and impact of Vdd on Pass Transistor Feed Inverters](image-url)
Level Restoring

![Level Restoring Diagram]

Level Restorer

![Level Restorer Diagram]

Level Restorer

![Level Restorer Diagram]
Level Restorer

Sizing of level restorer

Different level restoration leads to different logic families
Single-Ended Level Restoring

Lean Cell Library

Yano et al, CICC'94, JSSC 6/96
Various Logic Functions of the Lean Library

LEAP Comparison

3 input CMOS NAND
6 Xtrs, 329μ², 295pS, 0.91μW/MHz

3 input Y2 NAND
13 xtrs, 579μ², 465pS, 0.96μW/MHz

Overall 3 input functions

<table>
<thead>
<tr>
<th></th>
<th>3 input MJX</th>
<th>3 input NAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>avg cell size</td>
<td>1.92</td>
<td>3.09</td>
</tr>
<tr>
<td>avg input connections</td>
<td>5.11</td>
<td>11.4</td>
</tr>
<tr>
<td>avg cascade depth</td>
<td>2.23</td>
<td>3.08</td>
</tr>
</tbody>
</table>
Leap Comparison

Summary of the Comparison Results of Cells

<table>
<thead>
<tr>
<th></th>
<th>4-b Adder/Subtractor</th>
<th>7-ln, 4-Out Random Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CMOS</td>
<td>LEAP</td>
</tr>
<tr>
<td>Tr. Count /Cell</td>
<td>6.22</td>
<td>6.41</td>
</tr>
<tr>
<td>Gate Width / Cell</td>
<td>57μm</td>
<td>36μm</td>
</tr>
<tr>
<td>Net Count / Cell</td>
<td>2.9</td>
<td>4.7</td>
</tr>
<tr>
<td>Area / Cell</td>
<td>633μm²</td>
<td>571μm²</td>
</tr>
<tr>
<td>Delay Time / Cell</td>
<td>0.302ns</td>
<td>0.269ns</td>
</tr>
<tr>
<td>Power / Cell</td>
<td>45.7μW/MHz</td>
<td>45.2μW/MHz</td>
</tr>
</tbody>
</table>

LEAP Performance

LEAP faster than CMOS

V_C = 2.7 V_th

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Different Restoration Schemes

Swing-Restored Pass-Transistor Logic

Differential NMOS Logic Tree

Inputs

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Swing-Restored Pass-Transistor Logic

Gate Output

Swing Restoration

Gate Inputs

Complementary Control Variables

Complementary Pass Variables

Complementary Output

nMOS Pass Transistor Logic Networks

Parameswar, et al
CICC'94, JSSC 6/96

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