Other Level-Restoring Schemes

Energy Economized Pass-Transistor Logic

DCVS with Pass Gates (DCVS-PG)
Delay dependence on PMOS width and load, with NMOS constant
DCVSPG Latch

Transmission Gate Based Logic
Transmission Gate XOR

Transmission Gate Adder

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Transmission Gate Logic

Conditional Sum Adder

2-way MUXes

Rothermel, JSSC 89

TG Adder

- Conditional sum adder [Sklansky’60]
- Serial connection of transmission gates
- Chain length = $1 + \log_2 n$

Signal propagation

Parasitic capacitances

Input of the adder

Output

32 bit carry or sum signal

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TG Resistance

![TG Resistance Graph]

Delay in Transmission Gate Networks

![Networks Diagrams (a), (b), (c)]
Delay Optimization

- Delay of RC chain

\[ t_p = 0.69 \sum_{k=0}^{n} CR_{eq,k} = 0.69CR_{eq} \frac{n(n+1)}{2} \]

- Delay of Buffered Chain

\[ t_p = 0.69 \left[ \frac{CR_{eq}}{m} \cdot \frac{m(m+1)}{2} \right] + \left( \frac{n-1}{m} \right) t_{buf} \]

\[ m_{opt} = 1.7 \frac{t_{pbuf}}{CR_{eq}} \]

Double Pass-Transistor Logic (DPL)

AND/NAND

XOR/XNOR
Double Pass-Transistor Logic (DPL)

Same number of n- and p-channel devices

XOR

Sum

Designing DPL Gates

A B C D

A B C D

A B C D
Designing DPL Gates (2)

Applications of DPL

Full adder: 1.5ns 32-bit ALU in 0.25μm CMOS

Suzuki, ISSCC’93
JSSC 11/93
XOR Gate Comparison

<table>
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<th>CMOS</th>
<th>DPL</th>
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<td>Swing</td>
<td>0 ↔ (VCC - VIN)</td>
<td>0 ↔ VCC</td>
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4-bit Adder

[Diagram of 4-bit Adder]

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32-bit ALU

DPL Delay vs. Supply

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Applications of DPL

54x54bit DPL Multiplier in 4.4ns

Booth’s Encoder

Wallace’s tree

108-b CLA Adder

4:2 Compressor

Ohkubo, CICC’94, JSSC 5/95

4:2 Compressor in DPL