EE241 - Spring 2001
Advanced Digital Integrated Circuits

Lecture 8
Pass-Transistor Logic

Other Level-Restoring Schemes

Energy Economized Pass-Transistor Logic
DCVS with Pass Gates (DCVS-PG)
Delay dependence on PMOS width and load, with NMOS constant
DCVSPG Latch

Transmission Gate Based Logic
Transmission Gate XOR

Transmission Gate Adder
Transmission Gate Logic

Conditional Sum Adder

Conditional Cell

2-way MUXes

Rothermel, JSSC 89

TG Adder

- Conditional sum adder [Sklansky’60]
- Serial connection of transmission gates
- Chain length = 1+log₂n

Signal propagation

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TG Resistance

Delay in Transmission Gate Networks
Delay Optimization

- Delay of RC chain
  \[ t_p = 0.69 \sum_{k=0}^{n} CR_{eq} k = 0.69CR_{eq} \frac{n(n+1)}{2} \]

- Delay of Buffered Chain
  \[ t_p = 0.69 \left[ \frac{nCR_{eq}}{m} \frac{m(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right)t_{buf} \]
  \[ - 0.69 \left[ \frac{nCR_{eq}}{m} \frac{n(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right)t_{buf} \]

\[ m_{opt} = 1.7 \frac{t_{buf}}{CR_{eq}} \]

Double Pass-Transistor Logic (DPL)

- AND/NAND
- XOR/XNOR
Double Pass-Transistor Logic (DPL)

Same number of n- and p-channel devices

Designing DPL Gates
Designing DPL Gates (2)

Applications of DPL

Full adder:

1.5ns 32-bit ALU in 0.25µm CMOS

Suzuki, ISSCC’93
JSSC 11/93
**XOR Gate Comparison**

<table>
<thead>
<tr>
<th>Circuit</th>
<th>CPL</th>
<th>CMOS</th>
<th>DPL</th>
</tr>
</thead>
<tbody>
<tr>
<td>A XOR B</td>
<td></td>
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<table>
<thead>
<tr>
<th>Truth Table &amp; Operation</th>
<th>CPL</th>
<th>CMOS</th>
<th>DPL</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>XOR</td>
<td>Pass</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>B</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>B</td>
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Swing: $0 \leftrightarrow (V_{cc} - V_{th})$; $0 \leftrightarrow V_{cc}$; $0 \leftrightarrow V_{cc}$

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**4-bit Adder**

![4-bit Adder Diagram]

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32-bit ALU

DPL Delay vs. Supply

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Applications of DPL

54x54bit DPL Multiplier in 4.4ns

Booth’s Encoder

Wallace’s tree

108-b CLA Adder

Pass-transistor Multiplexer

Conditional Carry Selection (CCS)

Ohkubo, CICC’94, JSSC 5/95

4:2 Compressor in DPL

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Adder in DPL

4-bit adder

8-bit adder

Adder in DPL

108-bit final adder