### Types of Flip-Flops

**Latch Pair**

(Master-Slave)

- **D**
- **Clk**
- **Q**

**Pulse-Triggered Latch**

- **Data**
- **Clk**
- **L**

### Flip-Flop Delay

- Sum of setup time and Clk-output delay is the only true measure of the performance with respect to the system speed
- \[ T = T_{Clk-Q} + T_{Logic} + T_{setup} + T_{skew} \]
Master-Slave Latches

- Positive setup times
- Two clock phases:
  - distributed globally
  - generated locally
- Small penalty in delay for incorporating MUX
- Some circuit tricks needed to reduce the overall delay
Master-Slave Latches

Case 1: PowerPC 603 (Gerosa, JSSC 12/94)

T-G Master-Slave Latch

Feedback added for static operation
Unbuffered input
input capacitance depends on the phase of the clock
over-shoot and under-shoot with long routes
wirelength must be restricted at the input
Clock load is high
Low power
Small clk-output delay, but positive setup
Master-Slave Latches

Case 2: C²MOS

Feedback added for static operation
Locally generated clock
Poor driving capability
Robustness to clock slope

Pulse-Triggered Latches

First stage is a pulse generator
generates a pulse (glitch) on a rising edge of the clock
Second stage is a latch
captures the pulse generated in the first stage
Pulse generation results in a negative setup time
Frequently exhibit a soft edge property

Note: power is always consumed in the pulse generator
Pulse-Triggered Latches

Case 1: Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC’96

HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time
Hybrid Latch Flip-Flop

Flip-flops features:
- single phase clock
- edge triggered, on one clock edge

Latch features:
- Soft clock edge property
- brief transparency, equal to 3 inverter delays
- negative setup time
- allows slack passing
- absorbs skew
- Hold time is comparable to HLFF delay
- minimum delay between flip-flops must be controlled
- Fully static
- Possible to incorporate logic

Soft Edge Property

Also known as cycle borrowing, or slack passing
- In latch based designs, if longest path datum reaches latch before its setup time, clock skew does not affect cycle time
- If longest path reaches latch close to setup time, clock skew is directly subtracted from cycle time
- Flip-flop presents a ‘hard’ edge - no slack passing.
- HLFF is a compromise - has a controlled transparency period, that can absorb skew
- Price is paid in the hold time
Hybrid Latch Flip-Flop

Skew absorption

UC Berkeley EE241 Partovi et al, ISSCC’96

Pulse-Triggered Latches

Case 2: AMD K-7

Inputs are dynamically received
Clock edge is hard

To other flip-flops

Pulse-Triggered Latches

Case 3: Semi-Dynamic Flip-Flop (SDFF),
Sun UltraSparc III, Klass, VLSI Circuits'98

Pulse generator is dynamic, cross-coupled latch is added for robustness. Loses soft edge on rising transition
Latch has one transistor less in stack - faster than HLFF, but 1-1 glitch exists
Small penalty for adding logic

Pulse-Triggered Latches

Case 3: 7474, Texas Instruments’64
Karnaugh maps for signals $S$ and $R$

\begin{align*}
\begin{array}{|c|c|c|c|c|}
\hline
\text{Clk} & D & S & R \\
\hline
00 & x & 1 & 1 \\
01 & x & 1 & 1 & 1 \\
11 & x & 1 & 1 & 0 \\
10 & x & x & 0 & 0 \\
\hline
\end{array}
\end{align*}

\begin{align*}
\begin{array}{|c|c|c|c|c|}
\hline
\text{Clk} & D & S & R \\
\hline
00 & x & 1 & 1 \\
01 & x & 1 & 1 & 1 \\
11 & x & 1 & 1 & 0 \\
10 & x & x & 0 & 0 \\
\hline
\end{array}
\end{align*}

Pulse-Triggered Latches

DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when $\text{Clk} = 0$
After rising edge of the clock sense amplifier generates the pulse on $S$ or $R$
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges
Sense Amplifier-Based Flip-Flop

Flip-Flop Performance Comparison

Test bench

Total power consumed
internal power
data power
clock power
Measured for four cases
no activity (0000… and 1111…)
maximum activity (0101010..)
average activity (random sequence)

Delay is (minimum \(D-Q\)) \(Clk-Q + \text{setup time}\)

Stojanovic, Oklobdzija JSSC 4/99
Flip-Flop Performance Comparison

Delay vs. power comparison of different flip-flops
Flip-flops are optimized for speed with output transistor sizes limited to 7.5µm/4.3 µm
Total transistor gate width is indicated

Energy Consumption

- Always consume
  \[ E_{\text{CLK}} = E_{0,0} = E_{1,1} \]
- When Q : 1-0 or 0-1
  \[ E_{\text{int}} = E_{1,0} - E_{0,0} \]
- Only when Q : 0-1
  \[ E_{\text{ext}} = E_{0,1} - E_{1,0} \]

- Non-inverting Flops:
  \[ E_{\text{avg}} = E_{\text{CLK}} + \alpha \cdot E_{\text{ext}} + (1 - \alpha) \cdot E_{\text{int}} \]
- Inverting Flops:
  \[ E_{\text{avg}} = E_{\text{CLK}} + (1 - \alpha) \cdot E_{\text{ext}} + \alpha \cdot E_{\text{int}} \]

(\( \alpha \) - probability of D : 0-1)
Energy Dissipation

Comparison of Master Slave and Pulse-Triggered Flip-Flops

Resized for Energy/Delay

Local Clock Gating

'Clock on demand'
Flip-flop

UC Berkeley EE241
B. Nikolic