EE241 - Spring 2002
Advanced Digital Integrated Circuits

Lecture 5
Circuit Optimization for Speed

Reading

**Memory Architecture: Decoders**

- Input-Output (M bits)
- Storage Cell
- N Words => N select signals
- Too many select signals
- Decoder reduces # of select signals
  - \( K = \log_2 N \)

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**Array-Structured Memory Architecture**

- Problem: ASPECT RATIO or HEIGHT >> WIDTH
- Amplify swing to rail-to-rail amplitude
- Selects appropriate word
Memory Decoders

Collection of $2^m$ complex logic gates
Organized in regular and dense fashion

(N)AND Decoder

$\overline{WL_0} = A_0A_1A_2A_3A_4A_5A_6A_7A_8A_9$

$\overline{WL_{511}} = A_0A_1A_2A_3A_4A_5A_6A_7A_8A_9$

NOR Decoder

$\overline{WL_0} = \overline{A_0} + \overline{A_1} + \overline{A_2} + \overline{A_3} + \overline{A_4} + \overline{A_5} + \overline{A_6} + \overline{A_7} + \overline{A_8} + \overline{A_9}$

$\overline{WL_{511}} = \overline{A_0} + \overline{A_1} + \overline{A_2} + \overline{A_3} + \overline{A_4} + \overline{A_5} + \overline{A_6} + \overline{A_7} + \overline{A_8} + \overline{A_9}$

- Assume a 256 row decoder
- 8 address lines available in both true and complement values
- Each true/complementary input drives 128 complex AND gates.
- If it is a 256 x 256 memory, each AND gate drives a 256 cells
- Large fanout: $128 \times 256 \times \frac{C_{cell}}{C_{adr}}$
- Number of options how to implement
  » NAND8, or NAND4-NAND2, or NAND2-NAND2-NAND2 + inverters.
Memory decoders

- Number of stages = \( f(\text{fanout}) \)
- If \( \frac{C_{\text{cell}}}{C_{\text{adr}}} = 1 \), fanout = \( 2^{15} \)
- Optimal number of stages is \( \log_4 G 2^{15} \), which is not less than 7. If \( G \) is about 2 number of stages is 8.
- Is it better to use one large NAND8 and 7 inverters or NAND4, NAND2 and 6 inverters, or NAND2-NAND2-NAND2 and 5 inverters?
- Will it fit in the row pitch?
Divided Wordline

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Two-Level Decoder

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ALU Design

64-bit ALU

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ALU Design

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