Abstract— It is predicted that at the 90nm technology node, leakage power will surpass dynamic power. This poses several challenges to high-speed circuit designers. By the same token, the complexity of low power, low operating frequency designs is threatened more and more by static power dissipation concerns. It has been recently shown that if energy per operation (EOP) is used as an optimization metric, then for a given microarchitecture, an optimal choice of $V_{dd}$ exists. However, throughput constraints are considered in this design only a-posteriori, and are not included in the optimization problem. In this project, we aim to extend these results, bringing architectural considerations into the game.

The design and implementation of a digital filter, running at frequencies in the 1-10 MHz range, to be used as a decimator in a sigma-delta modulator, will be used as a case study. Different architectural solutions (FIR, IIR, serial) will be compared from these results, bringing architectural considerations into the game. Considerations to a dual-threshold, triple-well 90nm process.

Moving along the lines of [4], 9-stage ring oscillators with fan-in of 1 and fan-in of 4 have been used to characterize delay performance of the node across process and temperature variations. Some preliminary results from this analysis are reported here. Figures 2 and 1 respectively report $EOP-V_{dd}$ curves for parameter values $\alpha = 0.01, L_D = 10$ in the aforementioned technology. As apparent, optimal-EOP point shifts significantly both on the $x$ and the $y$ with temperature, while in case of different process corners, it is fairly constant in $x$ and varies by less than an order of magnitude in $y$. This behavior may be explained as follows. A reasonably accurate model for the delay of a digital gate operating at low supply voltages may be assumed to be the following

$$T_d = K_{fit} \cdot \frac{C \cdot V_{dd}}{I_0 \cdot e^{\frac{\sigma V_{fit} - V_{th}}{V_{dd}}} \cdot \frac{V_{dd}}{\gamma}}.$$

We express leakage as $I_{leak} = I_0 \cdot e^{\frac{\sigma V_{fit} - V_{th}}{V_{dd}}} \cdot \frac{V_{dd}}{\gamma}$, where $K_{fit}$ and $\gamma$ are fitting parameters, $C$ is the load capacitance, $I_0$ is a process dependent constant, $\sigma$ is the DIBL coefficient, and $\gamma$ is the subthreshold slope factor. Note the introduction of the factor $\gamma$, which is not included in either of [2], [3], [6], [4]. This factor accounts for the fact that the subthreshold slope factor used to estimate delay, due to gradual transition from weak to moderate inversion for supplies as low as about $V_{th} - 50mV$, to DIBL and to voltage dependent inversion layer capacitance [7].

For frequencies below $F_S$, we can express energy per operation as:

$$EOP = \left(\frac{C}{L_D} \cdot K_{fit} \cdot \frac{V_{dd}}{\gamma} \cdot \frac{1}{e^{\frac{\sigma V_{fit} - V_{th}}{V_{dd}}} \cdot \frac{V_{dd}}{\gamma} + C_t \cdot \alpha} \cdot V_{dd}^2 \right). \hspace{1cm} (1)$$

Now, assuming the dominant effect of process variations is the one on $V_{th}$, their impact is only shifting up or down by the first term by a factor that approaches 0 as $\gamma$ approaches unity. On the other hand, temperature variations impact both $V_{th}$ and $K \cdot T/q$. This turns into higher sensitivity of the optimal point to temperature than to process variations. An even more interesting question from a circuit design perspective is: given a technology that allows us to choose between two or three values of threshold voltage for the devices, under what conditions should high threshold and low threshold devices be used respectively? From the discussion above, it is clear that, given the competing role played by threshold voltage both in setting leakage power and delay, the answer is not obvious. For the present technology, the answer is reported in Figure 3. In this graph, parametric $F_S - EOP$ contours have been reported as $V_{dd}$ is swept. We can see that in fact, for moderate values of the switching activity $\alpha$, the $F_S - V_{dd}$ plane is divided into two well distinct regions, separated by a cross-over point ($F_S^*, EOP^*$). For frequencies below $F_S^*$, consider the constraints. In addition, we will also investigate scalability of such attempts as we increase the operating frequency beyond the 1-10Mhz range.

PROJECT OUTLINE

Comparing different architectural solutions on an energy-per-operation basis requires understanding of technological, circuitual and architectural issues. This is easily understood when looking at the equation expressing Energy per Operation (EOP):

$$EOP = V_{dd} \cdot I_{leak} \cdot T_d \cdot L_d + \alpha \cdot V_{dd}^2 \cdot C$$

Here $T_d$ is the delay time of one stage of logic, $L_d$ is the number of logic stages (logic depth) on the critical path, $C$ is the total switched capacitance, $I_{leak}$ is the total leakage current and $\alpha$ is the switching activity. Substituting $C = C_u \cdot \mathcal{N}_{gate}$ and $I_{leak} = I_u^{leak} \cdot \mathcal{N}_{gate}$, it becomes clear that in order to accurately explore the design space of a digital filter, we need to estimate the impact of decision at the technology/gate topology level (affecting $T_d$, $C_u$, $I_u^{leak}$); at the micro-architectural level ($\alpha$, $L_d$) and at the algorithm/filter structure level ($\mathcal{N}_{gate}$). All of these factors play an equally important role in driving the final implementation choice toward the energy-optimal point [1]. Therefore, this project addresses three major topics: technology characterization, micro-architecture modeling and hardware complexity estimation.

I. TECHNOLOGY CHARACTERIZATION

From the technology/gate topology side, significant work has already been done in [2], [3], [4], [5], [6]. However, this work has several limitations. In the first place, very little is said about temperature dependance of this optimal point [4] and nothing at all about the impact of process variations. We attempt to fill both these gaps in this project. Next, all of the aforementioned works deal with technologies at the 180nm node. We extend the
leakage plays a significant role, and performance is more cheaply achieved by the high-threshold option, even at the higher $V_{dd}$ required to meet the delay constraint. Above this frequency, switching power dominates, so it is better idea to use a low-threshold option, which allows operation at a lower $V_{dd}$. This point is made clear by Figure 4, which reports $V_{dd}$ versus delay for both the process options. Also, notice that, as expected, the crossover point does not exist for $\alpha = .01$, the HVT process being always better (leakage dominated scenario for each $V_{dd}$ value); while the trend reverses at $\alpha = 1$ (dynamic power dominated scenario). This graph gives a clear guide as to what process option to use, and namely, for realistic values of switching activities, the answer is always the high-V$\text{th}$ option.

Also, the effect of DTMOS operation is being investigated. This operation mode allows higher performance to be obtained for the same $V_{dd}$ as compared to conventional static CMOS at the cost of increased area and susceptibility to substrate noise.

II. MICRO-ARCHITECTURE MODELING

Parallelism and pipelining are established techniques to optimize energy for a given performance constraint by allowing slack for supply voltage reduction. However, it is still unclear if the same conclusion holds for design in the subthreshold region. Effects of these micro-architectural optimizations on the optimal-EOP point have not been investigated in detail, with the widest treatment being the one reported in [4].

Conventionally, an M-level pipelining system, exploits the reduction in $L_d$, equivalently a reduction in $C$ by a factor of M to allow for reduction in $V_{dd}$ required to charge the capacitances. Parallelism exploits the increased slack in clock period due to increased throughput to also reduce $V_{dd}$. This analysis takes into account only the dynamic part of the EOP equation, $C_d \cdot V_{dd}$. However, in the subthreshold region, as the ratio of leakage-to-active energy increases, careful analysis of the impact of pipelining and parallelism on subthreshold leakage energy dissipation is needed.

As reported in [4], the optimal-EOP point can be shifted to a lower or higher value depending of the ratio of the leakage-to-active energy. For a fixed active energy profile, any relative decrease in the leakage energy will shift the optimal-EOP point to a lower value. Likewise, for a fixed leakage component, any relative increase in dynamic energy will also shift the optimal-EOP point to a lower $V_{dd}$ value, albeit with a higher total energy per cycle.

As seen in the EOP equation above, the leakage energy component depends largely on $L_d$. Pipelining would be deemed
beneficial because $L_d$ decreases as the number of pipelined stages increases. We expect to see a reduction in the optimal-EOP point at lower $V_{dd}$ values. Further work will be carried out by simulations on pipelined and non-pipelined cascaded stages of XOR gates to validate this claim.

Another factor that contributes to the shifting of the optimal-EOP point is the activity factor $\alpha$ of a given architecture, namely the ratio of the capacitances being switched, $C_u$ to the total width of transistors allowed to leak, $W_{eff}$. Microarchitecture configurations that allow for idle leaky gates will increase the optimal-EOP point whereas configurations with higher $\alpha$ will yield lower EOP-points. No previous work has investigated and compared the relative $\alpha$s of pipelined and parallel architectures thus it is still unclear how parallel structures will contribute to the optimal-EOP optimization. We will attempt to study how pipelined and parallel configurations compare in terms of their $C_u/W_{eff}$ ratio and how their optimal-EOP point would compare one to the other.

III. HARDWARE COMPLEXITY ESTIMATION

Digital filters are typically implemented as FIR or IIR structures. FIR filter implementations are less sensitive to quantization errors, are guaranteed to be stable (the output is always bounded given a bounded input sequence), and can be designed to have linear output phase. IIR filters need to be designed carefully to avoid instability and are much more sensitive to quantization, but in contrast to FIR implementations, use much less taps. The sensitivity of IIR filters to quantization errors can be reduced by building it as a cascade of lower order filters instead of a single higher order filter.

Hardware complexity of a digital filter implementation depends on the number of taps and the bit-precision of the tap coefficients and the intermediate signals. Estimation of the number of taps and the tap coefficients (assuming infinite-precision) is simple—stable tools like MATHWORKS filter design and analysis tool, exist for filter-synthesis. Determining the bit-precision (for conversion from full-precision floating-point to fixed-point format) is still a subject of ongoing research. Traditional techniques for finding the right bit-precision rely on simulations, which, for complex systems, can take an unreasonably large time.

Carletta et al. [8] proposed an analytical technique for computing the required precision for signals in IIR filters. Their analysis uses the explicit knowledge of the system transfer function (in this case the transfer function of an IIR filter) to come up with bounds on quantization errors. The bit-precision is then chosen accordingly to meet the system specifications. The bit-precision of the intermediate signals is determined by computing their dynamic range which is obtained by propagating the maximum value of the inputs and the intermediate signals. This can sometimes be very conservative, resulting in a higher bit-precision than required.

Recently, Shi et al. [9] proposed a tool for automatic conversion of floating-point to fixed-point conversion (FFC) for digital signal applications. The task of FFC is posed as an optimization problem (i.e., minimize the hardware cost) subject to specification constraints (e.g., output signal-to-noise ratio).

The hardware complexity is modeled as a quadratic function of the number of fractional bits of the words. Simulations are used to obtain the specification constraints, which are essentially differences between the results from finite-precision and infinite-precision implementations. Simulations are also used to obtain dynamic range estimates.

Wu et al. [10] discuss the problem of dynamic range estimation (for linear systems) in more detail and propose an analytical technique, based on a mathematical tool called Karhunen-Loève Expansion (KLE). The signals and the intermediate results are modeled as random processes. KLE is applied to C program description of the system to obtain statistical information about the signals and the intermediate variables. This statistical information is then used to compute the bitwidths of the variables.

As a case study, we would compare FIR implementations with IIR implementations from an energy-per-operation perspective. In general, there are obvious hardware savings in using an IIR filter for a given frequency response when compared to FIR implementations. This is because the corresponding IIR filter will have a much lower order compared to the FIR filter. In fact, if output phase nonlinearity is not a problem, IIR filters are typically the choice for high-performance designs. However, this advantage is expected to be offset to a certain extent due the higher bit-precision needed for the IIR filter to guarantee stability and meet the signal-to-noise specifications. As part of hardware complexity estimation, a major portion will be estimating the required bit-precisions which we plan to do using a combination of the analytical and simulation-based techniques discussed above.

REFERENCES