Abstract—Aggressive device size scaling combined with Vdd and Vth scaling lead to increasing circuit performance variation. To meet performance expectations (such as low-power requirements), it may be expected that increasing circuit variability will lead to severe yield degradation. However, it has been shown [4] that despite the increasing variability of delay, slight sacrifices in yield can lead to large reductions in power consumption. However, this relationship has thus far only been demonstrated for a family of logic paths such as inverter chains and 4-bit adders implemented in various logic styles. To enable the robust low power digital circuit design, the performance variation of register is important as well.

Introduction

As technology scales, the process variation in VLSI manufacturing such as gate length, threshold voltage, and oxide thickness is increasing in proportion to the corresponding nominal value. Process variation, in conjunction with the additional variation inherent in circuit operational parameters such as the supply voltage and temperature, lead to a widening distribution of values for all performance metrics with technology scaling, particularly delay and power consumption of various logic paths and registers. Thus, although the scaling of technology and Vdd/Vth lead to an improved nominal circuit performance of a given circuit, it will reduce yield as the resulted performance variation also increases then more manufactured circuits fail to meet performance specifications. This tradeoff will only worsen with more aggressive scaling, and thus will become unacceptable to designers in the future unless effective robust design techniques are developed. The key to the successful development of these design techniques is a clear and thorough understanding of process variation and circuit operational parameters’ impact on performance of logic paths and registers.

Previous Research, Variation Modeling and Understanding

Early efforts to understand the effects of process variation on circuit performance have been based primarily on analysis of Monte Carlo simulation of various logic paths. This method models the sources of variation with mean and standard deviation of a given parameter. First, values of the various parameters under consideration are drawn from their respective distributions and assigned as device parameter values in a canonical test circuit. Then the canonical circuit is simulated using HSPICE or a similar circuit simulation engine, and the resulting performance metrics (propagation delay, power consumption) are measured. By repeating this sequence of selecting random device parameter values, assigning them to a canonical circuit, and measuring the performance of that resulting circuit, the variable nature of the circuit is captured.

This method has been used exhaustively in several published studies [1, 2]. In order to identify robust circuit design techniques that can minimize the impact of process variation on performance, analytical models must be developed from Monte Carlo analysis so that time-consuming simulations may be replaced by fast, direct computation. Orshansky et. al. developed a model to capture the dependence of delay distribution on CD(gate length) variation, expressed in the relation:
\[ \sigma_{\text{delay}} = 1.5^* (D/CD_0) \left[ \left( \frac{\sigma_{\text{CDcat}}^2}{\sigma_{\text{CDspat}}} + 0.28 \sigma^2 \right)/m + \sigma_{\text{CDspat}} \right]^{1/2}, \]

where \( D \) is the nominal circuit delay, \( CD_0 \) is the nominal gate length, and \( \sigma_{\text{CDcat}}, \sigma, \) and \( \sigma_{\text{CDspat}} \) are category dependent, random, and spatial components of gate length variation [3]. Although the model was shown to be accurate in Monte Carlo simulation, it is only marginally useful because no other sources of variation were taken into account. Thus, while the model captures the effect of CD variation alone nicely—useful here as motivation for a mask level correction to reduce CD variation—it does not offer the circuit designer much insight into robust design techniques.

P. Friedberg, R. Wang and et. al examined how different combinations of nominal supply voltage and threshold voltage (and the accompanying variations) and gate length variation simultaneously affect delay and power consumption of several logic paths in different logic styles [4], and confirmed that aggressive \( V_{dd} \) scaling comes at the cost of increased delay variability (as shown in Figure 1) and hence a degradation of circuit-level yield (as shown in Figure 2) also slight sacrifices in yield can lead to large reductions in energy consumption (as shown in Figure 3) for inverter chains, NAND chains and 4-bit adders, implemented in various logic topologies. It also showed that a similarly favorable yield-energy tradeoff exists across these circuit types and logic styles.
But no work was reported in the field of process variation and environmental variation’s impact on register performance in terms of setup time, C-Q delay and power. But register timing and power variations are as important as those of logic path in order to clock the digital blocks at even higher frequency with reasonable power in the presence of process and environmental variations, hence we need to evaluate and model register timing and power variations due to process and environmental variation and compare them with those of representative logic path.

**Progress and Proposed Study**

Algorithm and Perl script used to extract register timing parameters (Tsetup, Tc-q) and power have been developed and tested on multiplexer based master-slave register. The Monte Carlo simulation framework has been developed and is under testing.

In the next phase of this term project, the Perl script will be embedded into the Monte Carlo simulation framework to extract register performance variation due to process and environmental variation under different combinations of Vdd and Vth. The possibly different behaviors of multiplexer-based register, NMOS-only pass gate register, C²MOS register and TSPC register will be investigated. For the purpose of comparison, the corresponding performance variations of an inverter chain, as a representative of logic path, will also be extracted. All the simulations will be done in ST Microelectronics’ 90nm CMOS process. Analysis of delay variability due to Vdd and Vth scaling based on alpha power law [5,6] will also be presented to explain the Monte Carlo simulation results.

**REFERENCES**


