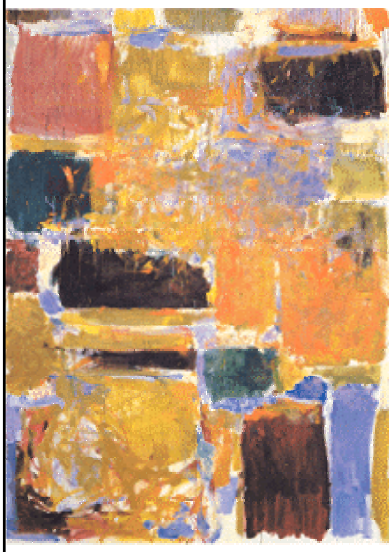


EE241 - Spring 2007

Advanced Digital Integrated Circuits

Lecture 23: Latches and Flip-Flops

Announcements

- Final exam on May 8 in class
- Project presentations on May 3, 1-5pm

Class Material

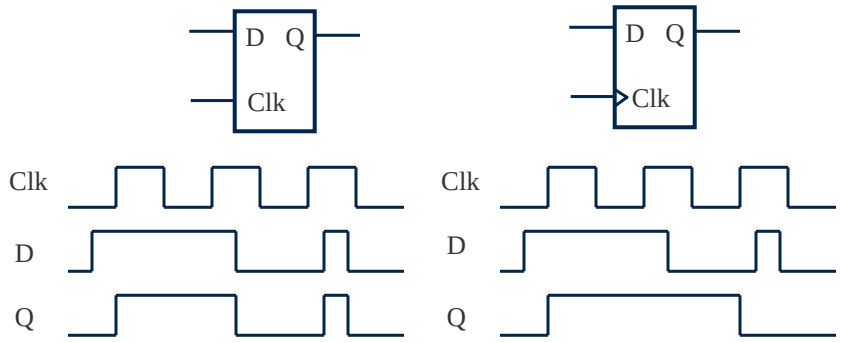
- Last lecture
  - SRAM
- Today's lecture
  - Latches and flip-flops

Latches: Reading

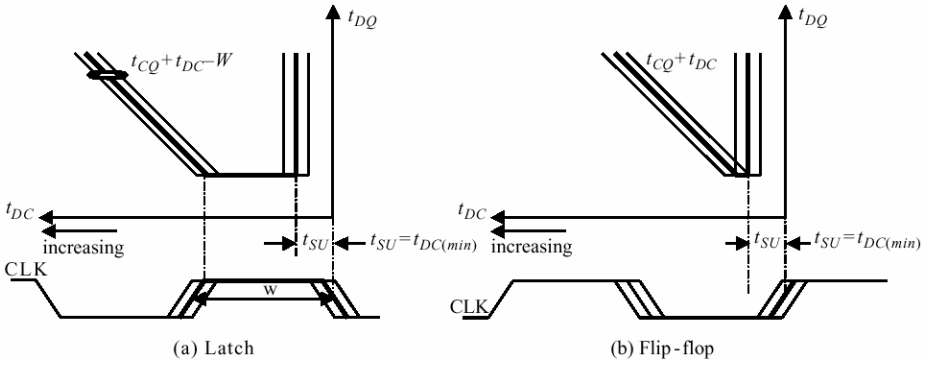
- Rabaey et al, Chapters 7 and 10
- Chapter 10 in Chandrakasan et al, by Partovi
- Stojanovic, Oklobdzija, JSSC 4/99

Latch vs. Flip-Flop

- Latch
  stores data when clock is low
- Flip-Flop (register)
  stores data when clock rises



Latch vs. Flip-Flop



Latch Pair vs. Flip-Flop

- Performance metrics
- Delay metrics
  - Delay penalty
  - Clock skew penalty
  - Inclusion of logic
  - Inherent race immunity
- Power/Energy Metrics
  - Power/energy
  - PDP, EDP
- Design robustness

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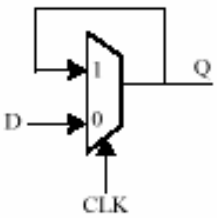
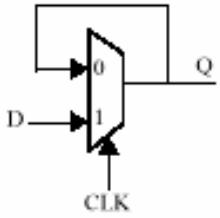
Latches

Negative latch
(transparent when CLK= 0)



Positive latch
(transparent when CLK= 1)



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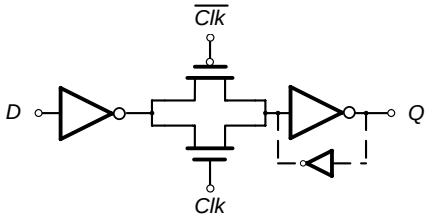
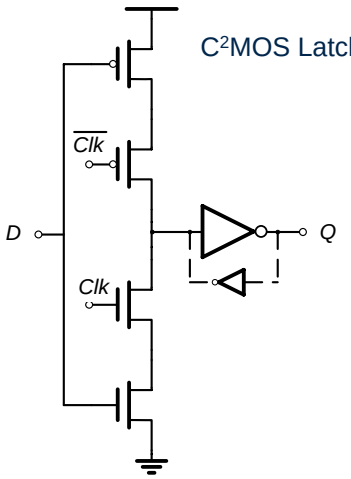
Latches

Transmission-Gate Latch



C²MOS Latch



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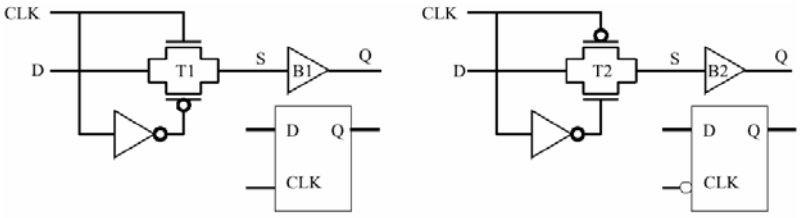
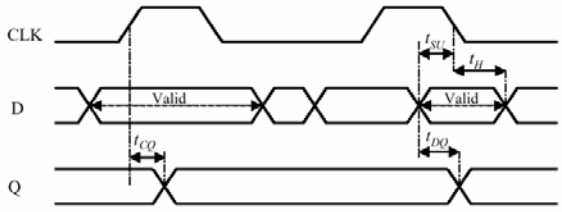
Latches



(a) The transparent high latch (THL)

(b) The transparent low latch (TLL)



(c) Timing waveforms for the THL

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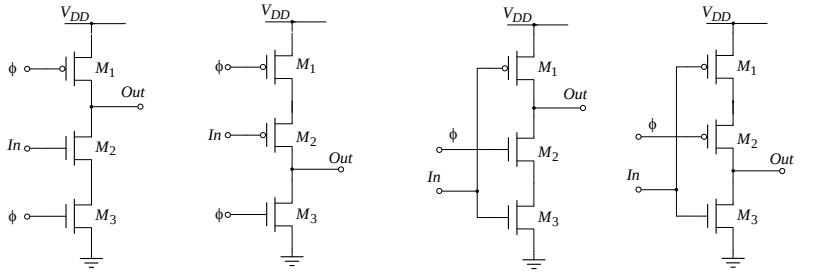
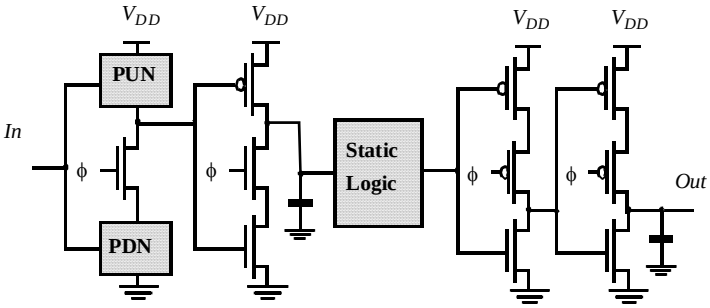
TSPC - True Single Phase Clock Logic



Precharged N | Precharged P | Non-precharged N | Non-precharged P

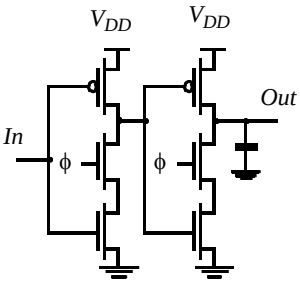
TSPC - True Single Phase Clock Logic



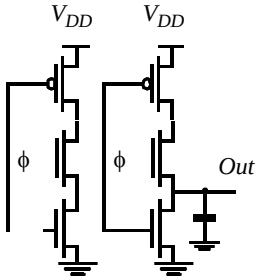
Including logic into the latch

Inserting logic between latches

Doubled TSPC Latches



Doubled n-TSPC latch



Doubled p-TSPC latch

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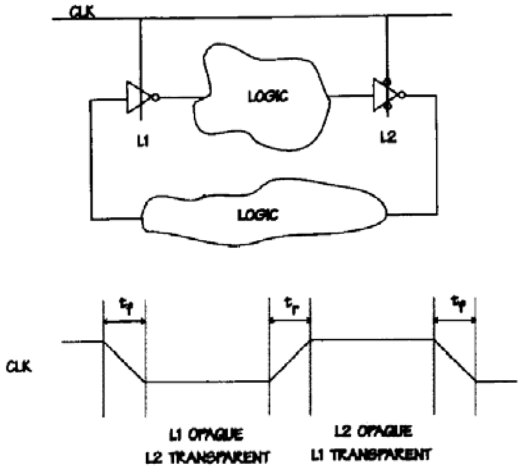
DEC Alpha 21064



Dobberpuhl, JSSC 11/92

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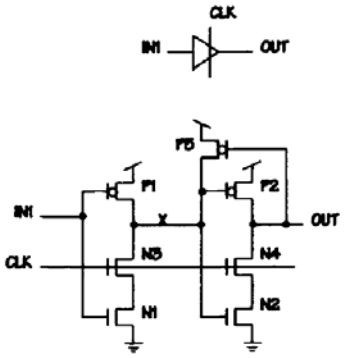
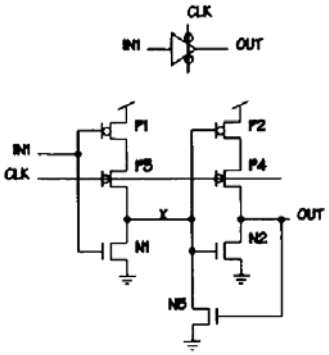
DEC Alpha 21064

L1:



L2:



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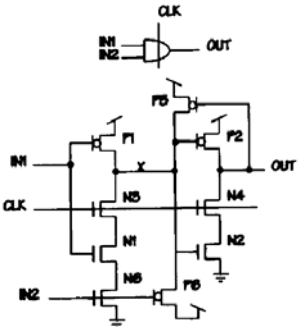
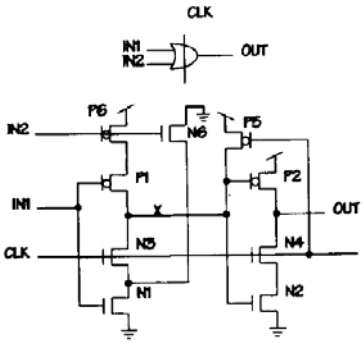
DEC Alpha 21064

Integrating logic into latches
• Reducing effective overhead





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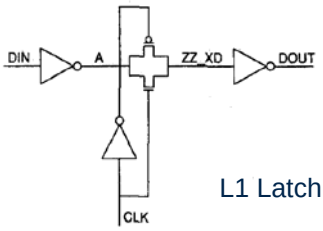
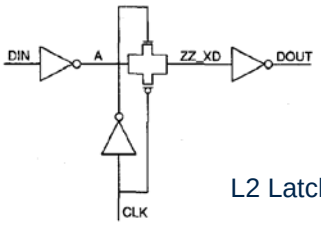
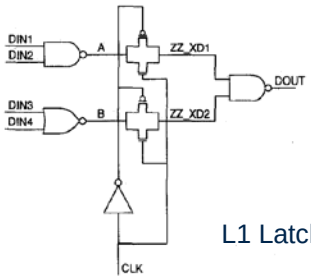
DEC Alpha 21164



L1 Latch



L2 Latch



L1 Latch with logic

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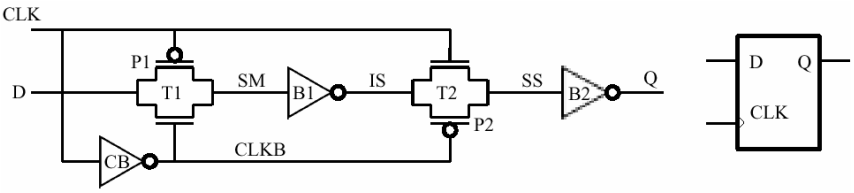
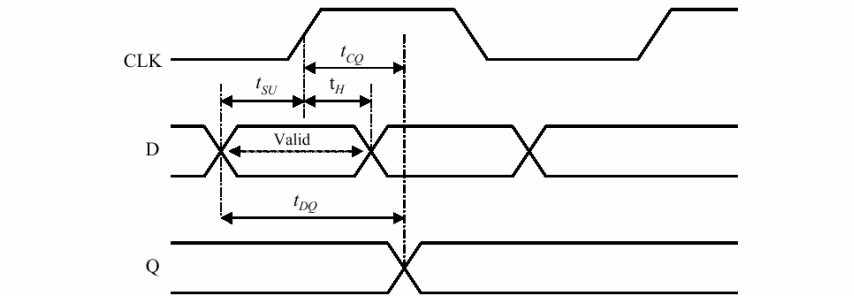
Latch Pair as a Flip-Flop





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Requirements for the Flip-Flop Design

- High speed of operation:
  - Small Clk-Output delay
  - Small setup time
  - Small hold time→Inherent race immunity
- Low power
- Small clock load
- High driving capability
- Integration of logic into flip-flop
- Multiplexed or clock scan
- Robustness
- Crosstalk insensitivity
  - dynamic/high impedance nodes are affected

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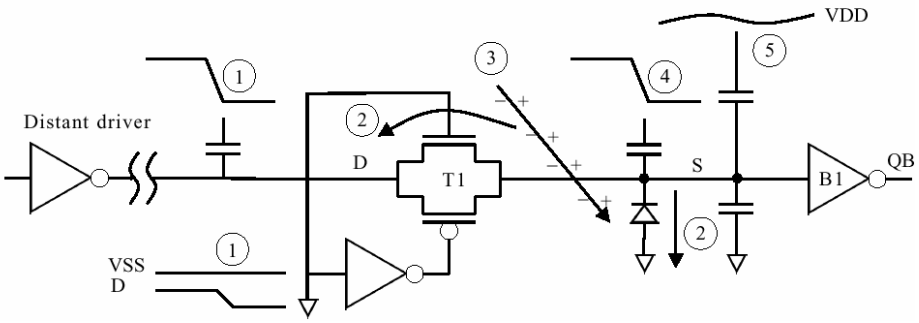
Sources of Noise

① Noise on input
② Leakage
③ α-Particle and cosmic rays
④ Unrelated signal coupling
⑤ Power supply ripple



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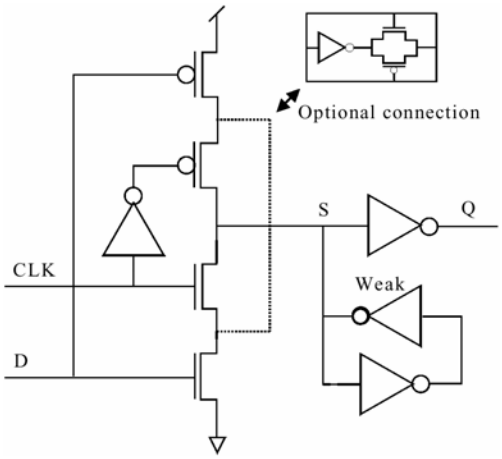
Gate Isolation



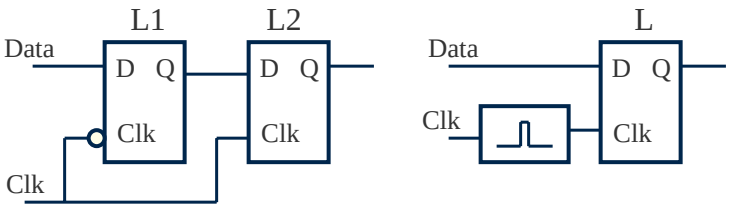
Flip-Flop Robustness

- Robustness of the storage node
- Input isolation
- Data stored statically, max resistance limit
- Min capacitance limit
- Preventing storage node exposure

Types of Flip-Flops

Latch Pair
(Master-Slave)

Pulse-Triggered Latch



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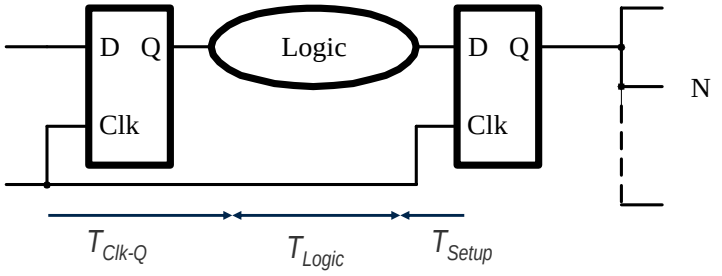
Flip-Flop Delay

- Sum of setup time and Clk-output delay is the true measure of the performance with respect to the system speed
- $T = T_{Clk\text{-}Q} + T_{Logic} + T_{setup} + T_{skew}$



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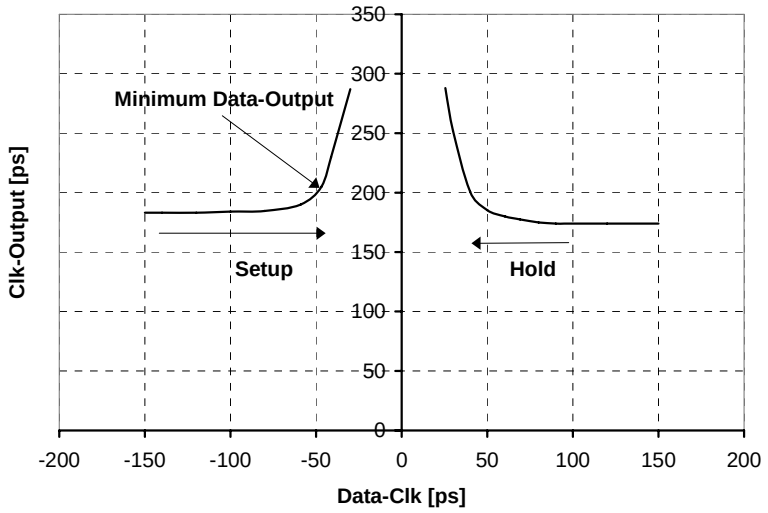
Delay vs. Setup/Hold Times



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Master-Slave Latch Pairs

- Positive setup times
- Two clock phases:
  - » distributed globally
  - » generated locally
- Small penalty in delay for incorporating MUX
- Some circuit tricks needed to reduce the overall delay

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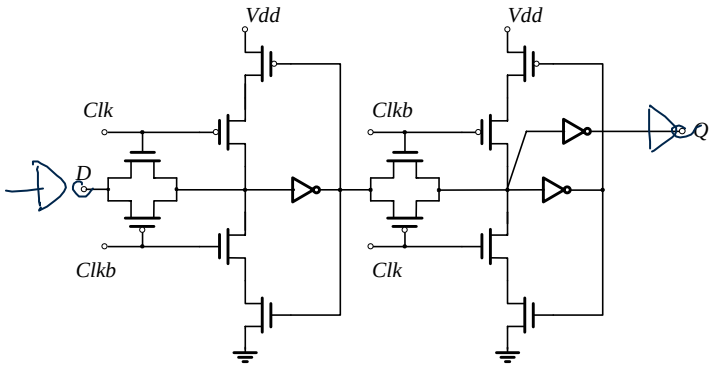
Master-Slave Latch Pairs

Case 1: PowerPC 603 (Gerosa, JSSC 12/94)



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T-G Master-Slave Latch

- Feedback added for static operation
- Unbuffered input
  - input capacitance depends on the phase of the clock
  - over-shoot and under-shoot with long routes
  - wirelength must be restricted at the input
- Clock load is high
- Low power
- Small clk-output delay, but positive setup

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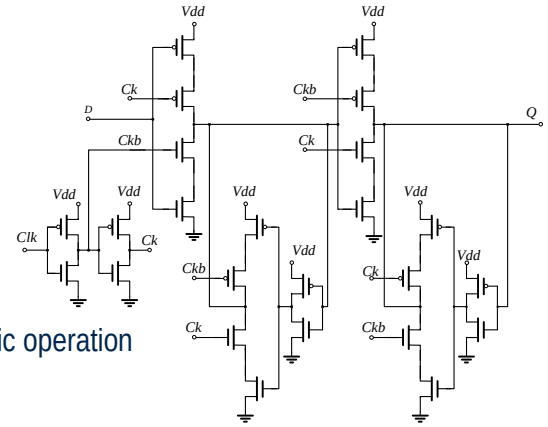
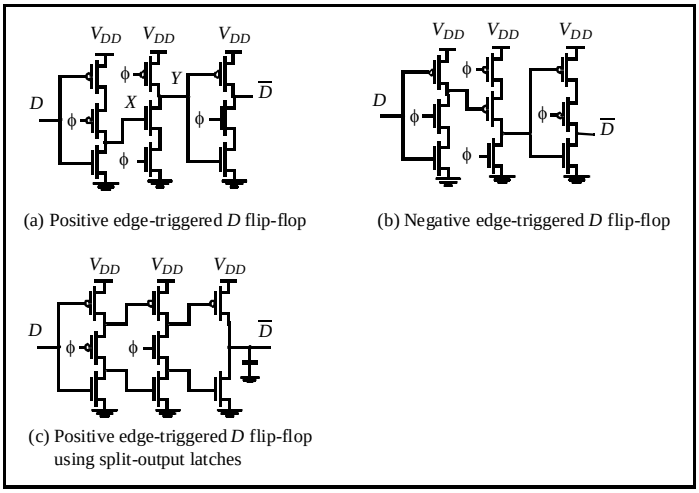
Master-Slave Latches

Case 2: C^{2}MOS



Feedback added for static operation
Locally generated clock
Poor driving capability

Master-Slave TSPC Flip-flops



(a) Positive edge-triggered *D* flip-flop

(b) Negative edge-triggered *D* flip-flop

(c) Positive edge-triggered *D* flip-flop using split-output latches

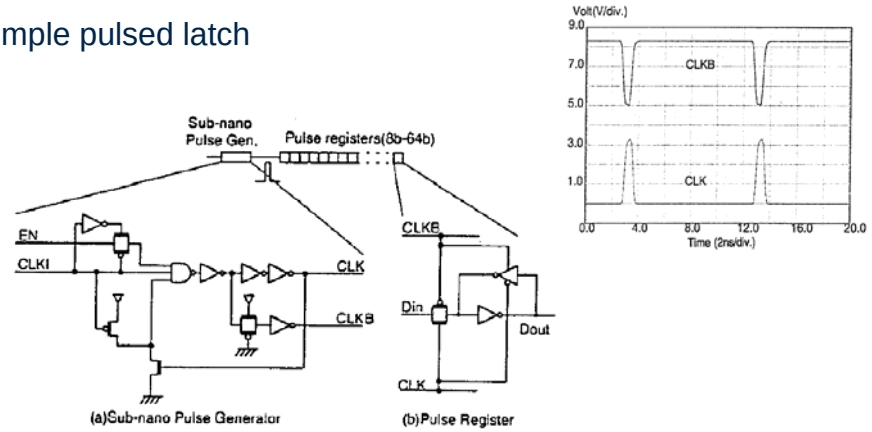
Pulse-Triggered Latches

- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property

- Note: power is always consumed in the pulse generator

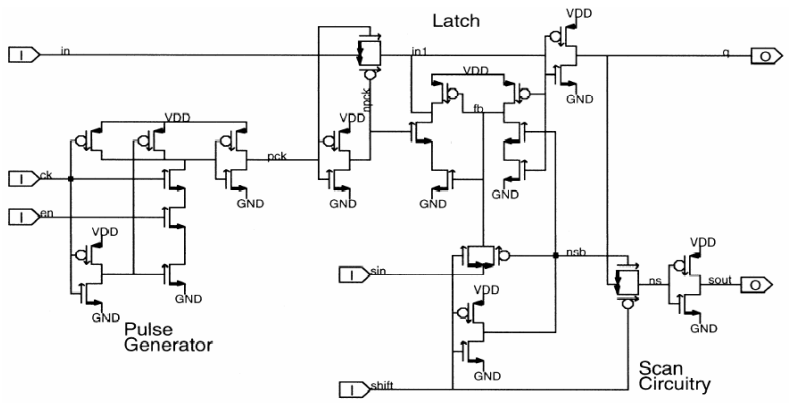
Pulsed Latch

Simple pulsed latch



Kozu, ISSCC'96

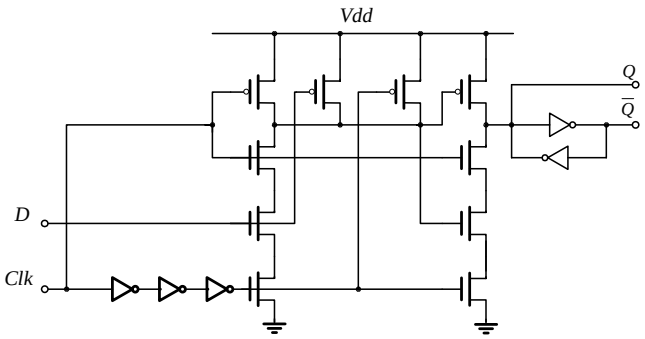
Intel/HP Itanium 2



Naffziger, ISSCC'02

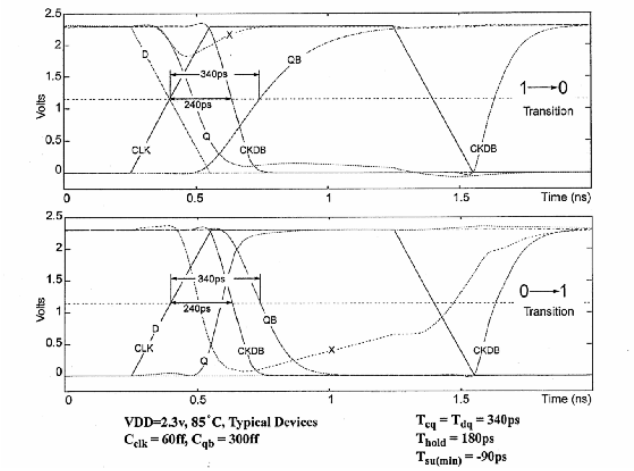
Pulse-Triggered Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96



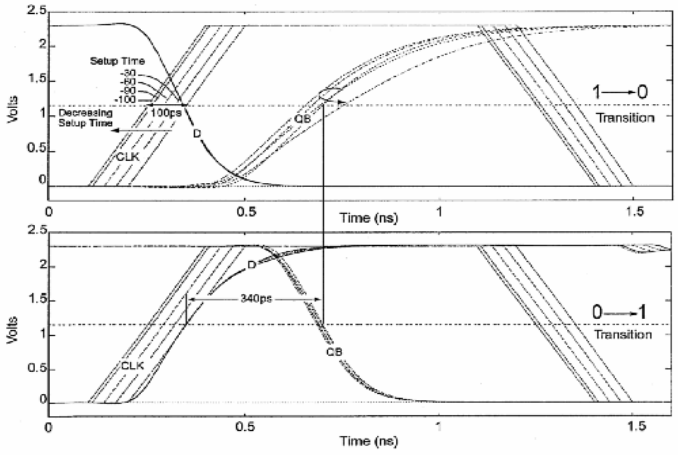
HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time



Hybrid Latch Flip-Flop

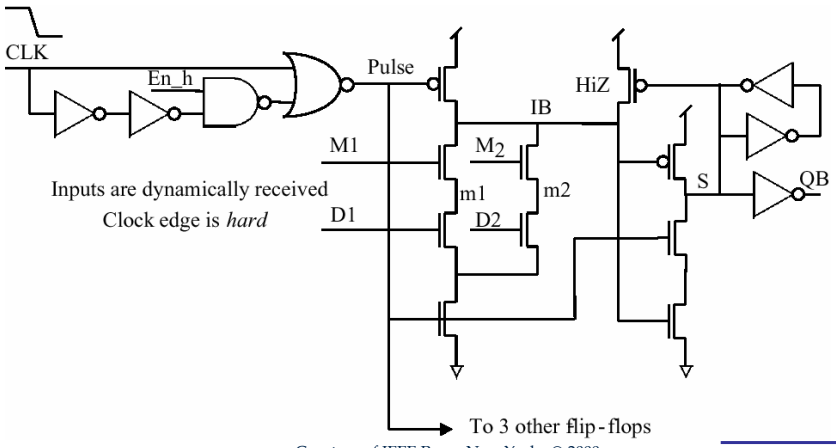
Skew absorption



Partovi *et al*, ISSCC'96

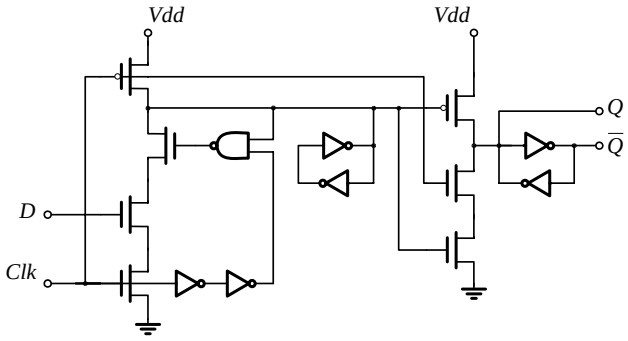
Pulse-Triggered Latches

AMD K-7



Pulse-Triggered Latches

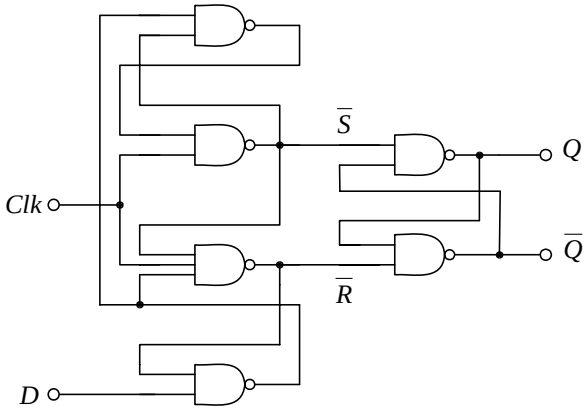
Semi-Dynamic Flip-Flop (SDFF),
Sun UltraSparc III, Klass, VLSI Circuits'98



Pulse generator is dynamic, cross-coupled latch is added for robustness. Loses soft edge on rising transition
Latch has one transistor less in stack - faster than HLFF, but 1-1 glitch exists
Small penalty for adding logic

Pulse-Triggered Latches

7474, from early 1960's



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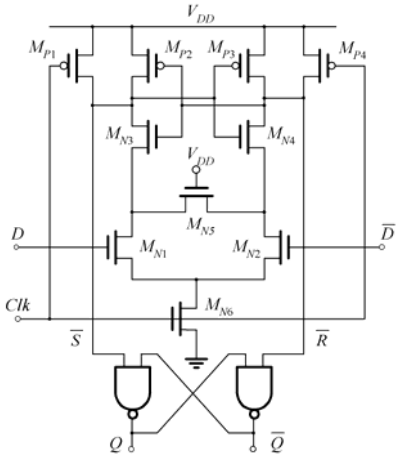
Pulse-Triggered Latches

Case 4: Sense-amplifier-based flip-flop, Matsui 1992.
DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when *Clk* = 0
After rising edge of the clock sense amplifier generates the pulse on *S* or *R*
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges



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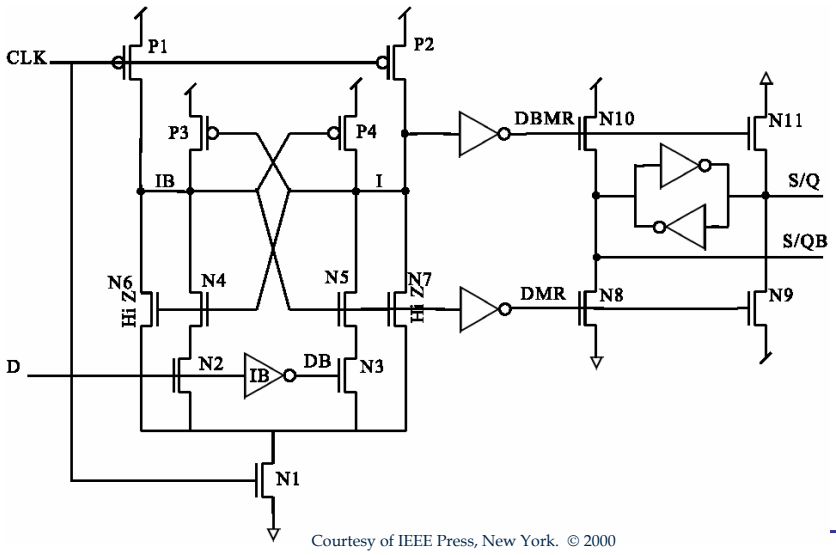
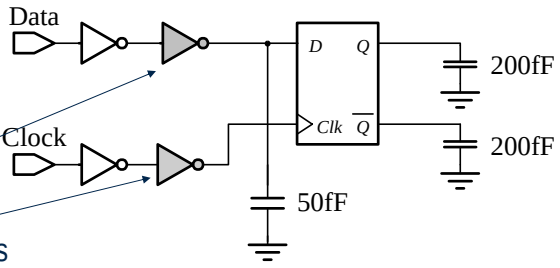
Sense Amplifier-Based Flip-Flop



Flip-Flop Performance Comparison

Test bench

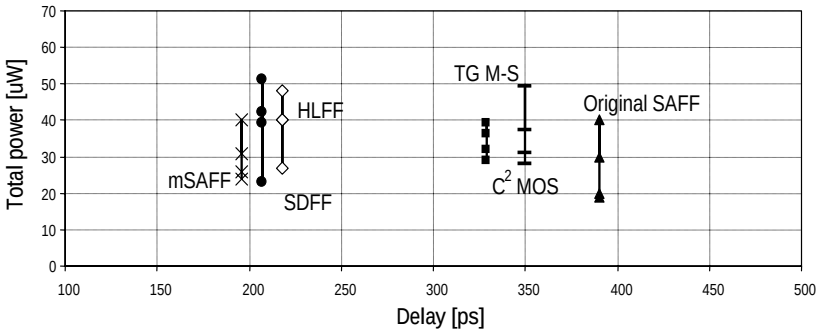
Total power consumed
internal power
data power
clock power
Measured for four cases
no activity (0000… and 1111…)
maximum activity (0101010..)
average activity (random sequence)



Delay is (minimum *D*-*Q*)
Clk-*Q* + setup time

Stojanovic, Oklobdzija JSSC 4/99

Flip-Flop Performance Comparison



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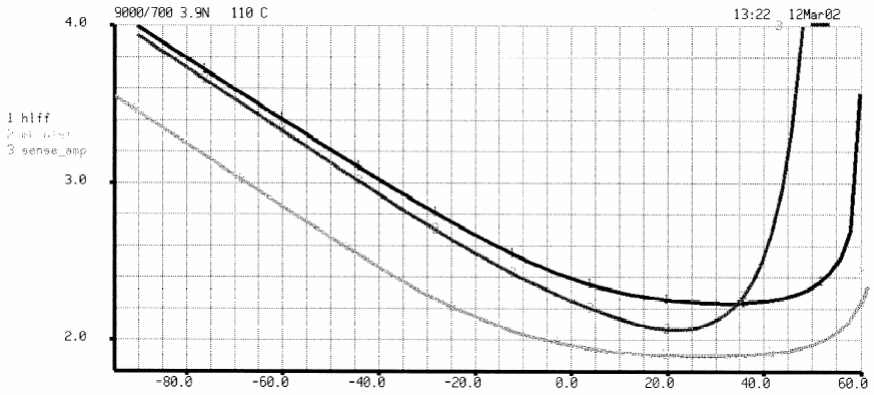
Sampling Window Comparison



Naffziger, JSSC 11/02

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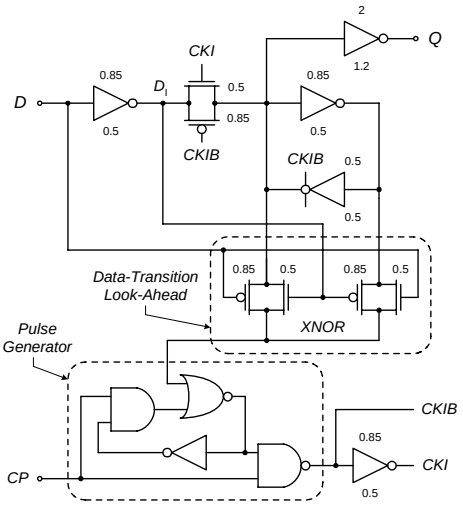
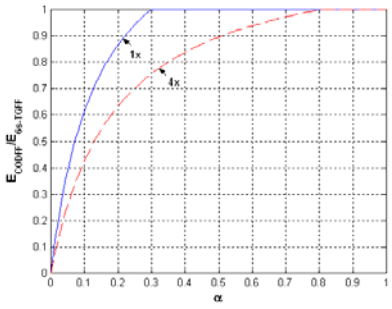
Local Clock Gating





'Clock on demand'
Flip-flop

Next Lecture

- Timing