Announcements

- **Homework 4**
  - Due April 15
  - Turn in to 253 Cory
- **No class next Thursday (April 17)**
Agenda

- Domino logic

Capacitive Coupling

[Diagram showing capacitive coupling with labels and symbols: \( \beta_{IN} \), \( IN \), \( C_{IN-CPL} \), \( \Delta V_{IN-CPL} \), \( M_{IN} \), \( IN2 \), \( C_{DYN-CPL} \), \( \Delta V_{DYN-CPL} \), \( M_{IN2} \), \( DYN \), \( OUT \), \( \rho_{OUT} \).]

Capacitive Coupling

Dynamic node: Static node:

![Diagram](image)

Lateral coupling: Shielding

![Diagram](image)
Minority Charge Injection

![Diagram of Minority Charge Injection](image1)

Supply Noise

![Diagram of Supply Noise](image2)
Domino Logic

Cascading Dynamic Gates

Only 0 → 1 Transitions allowed at inputs!
Cascading Dynamic Logic

DOMINO LOGIC

VDD

\( \phi \)

In\(_1\) In\(_2\) In\(_3\)

Out\(_1\)

M\(_p\)

PDN

Static Inverter with Level Restorer

Krambeck et al, JSSC 6/82

Krambeck et al, JSSC 6/82
Logical Effort

Inverter pair:

Skewed inverter pair:

Logical Effort

LE =
Designing with Domino Logic

Inputs = 0 during precharge

Can be eliminated!

Logical Effort

\[ LE = \]
Delayed Precharge

IBM’s 1GHz Processor
Example: 240ps adder

Kao, ISSCC'06

Layout Floorplan
Timing Diagram

Timing Diagram with waveforms for pc1, pc2, pc3, pc4, psel, H64, and H64'.

DUTY CYCLE:
- pc1: 24%
- pc2: 43%
- pc3: 53%
- pc4: 53%
- psel: 45%
- H64: Can only evaluate after inputs have settled

Domino Properties

- Logic evaluation propagates as falling dominoes
- Evaluation period determines the logic depth
- The nodes must be precharged during the precharge period (can limit the minimum size of PMOS)
- Inputs must be stable (or have only one rising transition) during the evaluation
- Gates are ratioless
- Restorer is ratioed
- All the gates are non-inverting
- Only one transition to be optimized
Logic Design Problem

- How to design an XOR/MUX without a complementary signal available?
- We need it in datapaths
- If the logic is followed by a flip-flop, or a latch with a hard edge, can use complementary or pass-transistor logic
- Domino logic is used with latches, and a new domino stage may follow the XOR

Solutions:
- Use dual-rail domino (dynamic CVSL)
- Violate some of domino rules (but still design a reliable circuit)
- Force a hard edge

Sum Implementation (1)

[Shimazaki, ISSCC’03]
Sum Implementation (2)

[Anders et al, ISSCC’02]

Sum Implementation (3): Strobing

[Park, VLSI’00]
Differential (Dual Rail) Domino

Dynamic CVSL (Clock CVSL) - Heller et al, ISSCC’84

Domino Techniques

Conditional keeper

Standard keeper

Conditional keeper

[Alvandpour, VLSI'01]
Other Dynamic Logic Styles

Self-Resetting Domino

- Signals exist as pulses, not levels
- Used in Pentium 4 (130nm generation)
**Pulsed Static CMOS**

RH – Reset high
RL – Reset low


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**Output-Prediction Logic**

Inverting logic:

Outputs-prediction logic:

McMurchie, et al, ICCD'2000
Output-Prediction Logic

NOR3:

Clocking:

McMurchie, et al, ICCD’2000

Output-Prediction Logic

NOR3 chain of 10:

Clock separation:
Multiple-Output Domino (MODL)

\[ F = F_1 F_2 \]

Hwang, Fisher, ISSCC’88

Lookahead Adder

Multiple Output Domino (MODL)
Compound Domino

Houston et al, U.S. Pat. 5,015,882
May 1991.

Next Lecture

- More dynamic logic
- Adders in power-performance space
Next Lecture

- Dynamic CMOS logic styles