1. SRAM Writeability

A circuit in Figure 1, connected to the standard bitlines attempts to enhance the write margin of standard 6T SRAM cells. The only inputs to the circuit are the input data (Din) and the write enable signal (WE). Draw a circuit that will enhance the SRAM writeability. You can use standard NMOS and PMOS transistors, and capacitors. Only regular supplies, V_{DD} and GND are available.

![Figure 1.](image)

Briefly describe the intended function of the circuit. Draw the detailed transistor-level circuit.

2. Latch timing parameters

Calculate the following delays for the latch from the Figure 2, relative to a unit inverter driving capacitance $C$:

a) Clock-to-output delay.
b) Data-to-output delay.
c) Setup time.
Both inverters are symmetrical and unit sized, with input capacitance equaling self-loading capacitance of $C$. Equivalent driving resistance of each inverter is $R$.

Transmission gate is sized to have the same equivalent resistance as the inverters.

Ignore the effect of signal slopes (except for the setup time calculation).

Clocks are ideal.

You can make a reasonable assumption on the dependence of the inverter’s equivalent resistance on VDD.

Setup time is defined at the point where the delay increases by 5% over its nominal value.

3. Timing

An example pipeline with a loop is shown in Figure 3. The input flip-flop launches the data at the rising edge of the flip flop, and the remaining sequential elements in the pipeline are transparent-high latches. The logic bubbles are designed with static logic.

Propagation delays are:

Flip-Flop: $t_{C-Q} = t_{\text{Setup}} = 200$ps

Latches: $t_{C-Q} = t_{D-Q} = 150$ps $t_{\text{Setup}} = t_{\text{Hold}} = 100$ps.

Logic delays: S1: 300ps, S2: 200ps, S3: 400ps, S4: 150ps.

Clock is ideal with 50% duty cycle.

Determine the maximum clocking speed in two cases:

a) Clock skew is zero.

b) Maximum clock skew is 100ps between any two storage elements (regardless of the phase of the clock).