Announcements

- Homework 1 due today
- Quiz #1 next Monday, March 7
### Outline

- Last lecture
  - SRAM
- This lecture
  - More SRAM

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### SRAM

**Read/Write Margins**
6T-SRAM Array Basics – Read Operation

Read Stability – Static Noise Margin (SNM)

- Read SNM is the contention between the two sides of the cell under read stress.

\[ \Delta V_{th} \propto \frac{1}{C_{ox} \sqrt{WL}} \]

E. Seevinck, JSSC 1987

Due to RDF
Read SNM - Measurements

Read margin and retention margin
[Bhavnagarwala, IEDM’05]

Read Stability – N-Curve

- A, B, and C correspond to the two stable points A and C and the metastable point B of the SNM curve
- When points A and B coincide, the cell is at the edge of stability and a destructive read can occur
Write Stability – Write Noise Margin (WNM)

- Writeability is becoming harder with scaling
- Optimizing read stability and writeability at the same time is difficult

A. Bhavnagarwala, IEDM 2005
Write Stability – BL/WL Write Margins

- Highest BL voltage under which write is possible when BLC is kept precharged
- Difference between VDD and lowest WL voltage under which write is possible when both bit-lines are precharged

Write Stability – Write Current (N-Curve)

- Minimum current logging into the storage node

C. Wann et al, IEEE VLSI-TSA 2005
The Conflict Between Read and Write

READ - OPTIMIZED SYSTEM

WRITE - OPTIMIZED SYSTEM

6-T SRAM Static/Dynamic Stability

- Read Margin
  - SNM: pessimistic
- Write Margin
  - WNM: optimistic
- Introduction of dynamic margins
Peripheral Circuits to Help SRAM

- Write assist techniques
- Read assist techniques
- Redundancy
- ECC
Multi-Voltage SRAM

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<thead>
<tr>
<th>Read</th>
<th>Write</th>
<th>Retention</th>
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<tr>
<td>Vmin</td>
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<td>Vmin (L)</td>
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<td>Vmin</td>
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<td>Vmax</td>
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<td>Vmin</td>
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Array Adjustments

Array back bias, to compensate for systematic variations

S. Mukhopadhyay, VLSI 2006
Dynamic $V_{DD}$ Implementation

- VCC selection is along column direction to decouple the read & write

Zhang, ISSCC'05

Capacitive Write Assist

- The collapsed drawing of the actual wave form of the selected column immediately after starting access cycle.

S. Ohbayashi, VLSI 2006
Write/Read Assist

H. Pilo, VLSI 2006

Pulsed WL/BL

M. Khellah, VLSI 2006
Negative BL

Nii, VLSI'08

Next Lecture

- SRAM design techniques