Announcements

› Homework 2 due next week
› Quiz #1 today
Outline

› Last lecture
  › SRAM operation, static margins

› This lecture
  › Finish static margins,
  › Dynamic margins
  › Start assist techniques

SRAM

C. Static Read/Write Margins
(continued)
Write Stability – Write Noise Margin (WNM)

- Writeability is becoming harder with scaling
- Optimizing read stability and writeability at the same time is difficult

A. Bhavnagarwala, IEDM 2005

Write Stability – BL/WL Write Margins

- Highest BL voltage under which write is possible when BLC is kept precharged
- Difference between VDD and lowest WL voltage under which write is possible when both bit-lines are precharged
Write Stability – Write Current (N-Curve)

- Minimum current into the storage node

C. Wann et al, IEEE VLSI-TSA 2005
The Conflict Between Read and Write

6-T SRAM Static/Dynamic Stability

- Read Margin
  - SNM: pessimistic
- Write Margin
  - WNM: optimistic
- Introduction to dynamic margins
D. Dynamic Margins

Dynamic Write Stability

- \( T_A < T_{\text{write}} < T_B \)
- \( T_{\text{write}} = \text{dynamic write stability} \)
- Static margins are optimistic

Khalil, TVLSI'08
Dynamic Read Stability

- $T_A < T_{\text{read}} < T_B$
- $T_{\text{read}} =$ dynamic read stability
- Static margins are pessimistic

Khalil, TVLSI '08

Dynamic Read Access

- $T_A < T_{\text{access}} < T_B$
- $\text{PD}_1$ and $\text{PG}_1$ are critical

Khalil, TVLSI '08
$V_{Th}$ Window

Assuming global spread

Yamaoka, ISSCC’05

SRAM

E. Assist Techniques
Peripheral Circuits to Help SRAM

- Write assist techniques
- Read assist techniques
- Redundancy
- ECC

Multi-Voltage SRAM

<table>
<thead>
<tr>
<th></th>
<th>Read</th>
<th>Write</th>
<th>Retention</th>
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<tr>
<td>Periphery</td>
<td>Vmin</td>
<td>Vmin</td>
<td>Vmin</td>
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<tr>
<td>BL Precharge</td>
<td>Vmin (H)</td>
<td>Vmin (L)</td>
<td>Vmin</td>
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<tr>
<td>WL</td>
<td>Vmin</td>
<td>Vmax</td>
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<tr>
<td>Cell $V_{DD}$</td>
<td>Vmax</td>
<td>Vmin</td>
<td>Vmin</td>
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</tbody>
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$V_{SS}$
Array Adjustments

Array back bias, to compensate for systematic variations

May be useful in technologies with strong body effect

S. Mukhopadhyay, VLSI 2006
Dynamic \( V_{DD} \) Implementation

- VCC selection is along column direction to decouple the read & write

Zhang, ISSCC'05

Floating VDD Technique

- W/o second supply

Yamaoka, ISSCC'04
Collapsing V\textsubscript{DD} Technique

E. Karl, ISSCC'12
Negative BL

Nii, VLSI'08

Negative BL

Arsovski, ISSCC’11
BL Stability Assist

- Arsovski, ISSCC’11

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WL Underdrive

- Sensing appropriate WL voltage

- Carlson, CICC’08
- Nho, ISSCC’10
Capacitive Write Assist

Write/Read Assist
Pulsed WL/BL

![Diagram of Pulsed WL/BL]

M. Khellah, VLSI 2006

Next Lecture

- Continue with SRAM