Announcements

› Sign up for Piazza if you haven’t already
Assigned Reading

  - Just the scaling principles

Outline

- Scaling issues
- Technology scaling trends
- Features of modern technologies
  - Lithography
  - Process technologies
Part 1: Technology

A. Scaling Trends
Transistor Counts

Transistor Counts in Intel's Microprocessors

Doubles every 2 years

Frequency

Frequency Trends in Intel's Microprocessors

Has been doubling every 2 years

Nearly flat
Power Dissipation

Power Trends in Intel’s Microprocessors

Has been > doubling every 2 years

Has to stay ~constant

B. Scaling Issues
CMOS Scaling Rules

SCALING:
Voltage: $V/\alpha$
Oxide: $t_{ox}/\alpha$
Wire width: $W/\alpha$
Gate width: $L/\alpha$
Diffusion: $x_d/\alpha$
Substrate: $\alpha^*N_A$

RESULTS:
Higher Density: $\sim \alpha^2$
Higher Speed: $\sim \alpha$
Power/ckt: $\sim 1/\alpha^2$
Power Density: $\sim$Constant


CMOS Scaling

› Two 30nm transistors (then and now)
Transistor Scaling

“Contacted gate pitch”

Shrink by 30%

Gate pitch scales 0.7x every node
Intel 22nm: contacted gate pitch 90nm

Ideal vs. Real Scaling

Leakage slows down $V_{Th}$, $V_{DD}$ scaling
Technology Flavors

LP keeps drain leakage constant

32nm Technology Flavors (Intel)

<table>
<thead>
<tr>
<th>Transistor Type</th>
<th>Logic (option for HP or SP)</th>
<th>Low Power (option for 1.8 or 3.3 V)</th>
<th>HV I/O (option for 1.8 or 3.3 V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOT (nm)</td>
<td>0.95</td>
<td>0.95</td>
<td>4</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>0.75/1</td>
<td>0.75/1.2</td>
<td>1.5/1.8</td>
</tr>
<tr>
<td>Pitch (nm)</td>
<td>112.5</td>
<td>126</td>
<td>min. 338</td>
</tr>
<tr>
<td>Lgate (nm)</td>
<td>30</td>
<td>46</td>
<td>&gt;140</td>
</tr>
<tr>
<td>NMOS Idsat (mA/um)</td>
<td>1.53 @ 1V</td>
<td>0.68</td>
<td>1.8 V</td>
</tr>
<tr>
<td>PMOS Idsat (mA/um)</td>
<td>1.23 @ 1V</td>
<td>1.8 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Ioff (nA/um)</td>
<td>100</td>
<td>0.03</td>
<td>&lt;0.01</td>
</tr>
</tbody>
</table>
Lg, R, C scaling

- With scaling L, need to scale up doping - scale junction depth (control leakage) – S/D resistance goes up
- External resistance limits current

\[ I_D \approx \frac{V_{DS}}{R_{\text{channel}} + R_{\text{ext}}} \]

Parasitic Capacitance Scaling

Reality: Overlap + fringe can be 50% of \( C_{\text{channel}} \) in 32nm
C. 32/28nm Technology Features

Technology Features

› Lithography implications (this lecture)
  › Restrictions on design
  › Implications on design variability
› FEOL features (next lecture)
› Models
EE 141 Technology vs. 32/28nm

FEOL  
0.25μm features  
Lg ~ 240nm  
248nm lithography  
No OPC, liberal design rules  
SiO₂ oxide, 3.5nm  
10⁶ dopant atoms  
LOCOS  
Nobody knew what 'strain' is  
Velocity saturated  
No SD leakage  
No gate leakage  
One transistor flavor

BEOL  
Al interconnect  
SiO₂ ILD  
4-5 M layers  
No CMP, no density rules

FEOL  
32nm technology  
Lg ~ 30-35nm  
193nm immersion lithography  
OPC, restricted design rules  
Hf-based dielectric  
~10¹⁰ dopant atoms  
STI  
Strained silicon in channel  
Velocity saturated  
lₜ₉₅₉₅ ≈ 100nA/µm  
Low gate leakage  
Many transistor flavors

BEOL  
Cu interconnect  
Lo-k ILD  
8-11 M layers  
CMP, density rules

Step-and-Scan Lithography
Lithography Scaling

Nominal feature size scaling

EUV – Technology of the future (forever)?

Sub-Wavelength Lithography

› Light projected through a gap

193nm light

Mask

Constant pitches / Forbidden pitches
Sub-Wavelength Lithography

\[ CD = k_i \frac{\lambda}{NA} \]

- **Decrease \( \lambda \)**
  - Presently: 193 nm (ArF excimer laser)
  - (Distant?) future: EUV

- **Increase \( NA = n \sin \alpha \)**
  - Maximum \( n \) is 1 in air
  - Presently: \( \sim 0.92-1.35 \)
  - Immersion

- **Result: Shrinking \( k_1 \)**
  - Presently: 0.35 – 0.4
  - Theoretical limit: 0.25

\[ CD_{\text{min}} = k_i \frac{\lambda}{NA} = 0.25 \frac{193 \text{nm}}{0.92} = 50 \text{nm} \]

45nm technology beyond resolution limit