Announcements

- Office hour on Monday moved to 1-2pm and 3:30-4pm
- Final exam next Wednesday, in class
  - Open book open notes
- Project reports due May 3, presentations are on May 6 at BWRC
Project reports

- 6 pages, two columns
- Content
  - Title, authors, contact
  - Abstract
  - Intro
  - Background
  - Key idea – what did you do?
  - What do you base your results on? What did you implement?
  - Results
  - Conclusion

Presentations
- In BWRC on May 6
- 1-4:30pm
- 6min + 4min/person slots
  (i.e. single person: 10min, 3 people projects: 18min)

Outline

- Last lecture
  - Clock generation
  - Phase locked loops
- This lecture
  - Continue PLL components
6. Clocks and Supplies  
C. PLL Components

Charge Pump

- Converts PFD digital \( UP/DN \) signals into charge
- Charge is proportional to duration of \( UP/DN \) signals
  \[
  Q_{cp} = I_{UP} t_{UP} - I_{DN} t_{DN}
  \]
- The LPF converts integrates currents
- Charge pump requirements:
  - Match currents \( I_{UP} \) and \( I_{DN} \)
  - Reduce control voltage coupling
  - Supply noise rejection, PVT insensitivity
    (Simple or bandgap biased)
Charge Pump: Better Switches

- Unity-gain buffer controls the voltage over switches
- Current mirrored into $I_{up}/I_{dn}$

Loop Filter

- Integrates charge-pump current onto $C_1$ cap to set average VCO frequency ("integral" path).
- Resistor provides instantaneous phase correction w/o affecting avg. freq. ("proportional" path).
- $C_3$ cap smooths IR ripple on $V_{ctl}$
- Typical value $R_{lpf}$ in kΩ
Loop Filter: Dual CP

- Transformation into PI

- Dual charge pump architecture

![Diagram of Dual Charge Pump Architecture]

Maneatis, JSSC 12/96

Low-Pass Filter Smoothing Cap (C₃)

- "Smoothing" capacitor on control voltage filters CP ripple, but may make loop unstable
- Creates parasitic pole: \( p = 1/(R \cdot C_3) \)
- \( C_3 < 1/10 \cdot C_1 \) for stability
- \( C_3 > 1/50 \cdot C_1 \) for low jitter
- Smoothing cap reduces "IR"-induced VCO jitter to < 0.5% from 5-10%
- \( f_{vco} = K_{vco} \cdot I_{cp} \cdot T_{err}/C_3 \)
- Larger \( C_3/C_1 \) increases phase error slightly

Fischette, ISSCC'04
Filter Capacitors

- Traditionally thin gate capacitance has been used
  - Below 130nm gate leakage is a problem
  - $C_1$ in the range of tens of pF
- Alternative: thick oxide or metal cap
  - Area penalty

Variable Delay Elements

- Need:
  - a delay element
  - a method to vary the delay
- Delay elements
  - inverter
  - source-coupled amplifier
- Methods to vary delay
  - multiplexing a tapped delay line
  - varying the power supply to an inverter chain
  - varying the capacitance driven by each stage
  - varying the resistive load of a source-coupled amplifier
- Characterized by
  - max and min delay
  - typically a 2:1 throw
  - stability (jitter)

$\text{[Dally]}$
Variable Delay Elements

- Single-ended vs. differential
- In CMOS inverter 1% of change in supply changes the delay by 1%
  (keep this in mind when using clock buffering)
- Current starved inverters and RC-loaded inverters are worse than 1%-for-1%.
- Improve by adding stabilization

Example VCO

- Ring-oscillator-based VCO: RC loaded
- Ring-oscillator-based VCO: Current-starved

Hudson, JSSC’88
Jeong, JSSC’87
Regulated Delay Line

- Sidiropoulos’00

VCO: simple differential delay

- Change current
- Or better: Resistances
- Need linear, variable resistors
Delay Elements

Maneatis, JSSC’95

6. Clocks and Supplies
D. Digital PLL in Practice
Digital PLL

- Replace analog functions with digital equivalents

![Digital PLL Diagram]

- Digitally-controlled oscillator (DCO)

Practical Digital PLL

- In IBM Power7 processor, per each core

Tierno, VLSI’10
One PLL with multiple DLLs

- Single PLL, and two cores vary frequency through digital frequency dividers (DFDs) and DLLs

Clock and Supply

- Large digital systems can have large voltage transients
  - Can we filter impact of voltage on a clock generator?

Kurd, JSSC’09
IBM Power7, with one PLL per core

Lefurgy, MICRO’11
6. Clocks and Supplies
E. Supply Voltage

Supply Generation

- **Linear**
  - Series or shunt
  - Linear regulation
  - Quiet
  - Inefficient (unless Vin-Vout is small)

- **Switching (Capacitive)**
  - Limited efficiency
  - Poor regulation
  - Voltage ripples

- **Switching (Magnetic)**
  - Efficient
  - Require external components
  - Noisy
Power Delivery

Typical model

![Typical model diagram](image)

Wong, JSSC'06

Next Lecture

- Finish supply voltage
- Wrap up