EE241 - Spring 2013
Advanced Digital Integrated Circuits

Lecture 3: Features of Modern Technologies

Agenda

- Previous lecture
  - Scaling issues
  - Technology scaling trends
  - Features of modern technologies

- Today’s lecture
  - Finish lithography
  - Typical 32/28nm process
Pop Quiz

According to Dennard’s 1974 paper when the scaling stops?

C. 32/28nm Technology Features - Lithography
Litho: How to Enhance Resolution?

1. Immersion
2. Off-axis illumination
3. Resolution enhancement/Optical proximity correction
4. Restricted design rules (RDR)
5. Phase-shifting masks
6. Double patterning

Litho (1): Immersion

› Project through a drop of liquid
› $n_{\text{water}} = 1.47$

$CD_{\text{min}} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193\text{nm}}{1.35} = 35\text{nm}$
Litho (2): Illumination

- Regular Illumination
- Many off-axis designs (OAI)
  - Annular
  - Quadrupole / Quasar
  - Dipole

- Amplifies certain pitches/rotations at expense of others

Based on A. Kahng, ICCAD’03

Litho (3): Resolution Enhancement

- NO OPC
- OPC
- Endcap enlarged from 180 to 120nm
- C120 SRAM 2.5μm²
- C090 SRAM 1.15μm²
- C065 SRAM 0.525μm²

J. Hartmann, ISSCC’07
Optical Proximity Correction (OPC) modifies layout to compensate for process distortions

- Add non-electrical structures to layout to control diffraction of light
- Rule-based (past) or model-based
Litho (4): Restricted Design Rules

- Standard cell
- Regular layout
- STI isolation
- Also: note poly density rules

J.Hartmann, ISSCC'07

Litho (5): Phase-Shift Masks

- Phase Shifting Masks (PSM)
  - Creates interference fringes on the wafer → Interference effects boost contrast → Phase Masks can make extremely small lines

- Conventional mask:
  - Glass
  - Chrome
  - Electric field at mask
  - Intensity at wafer

- Phase shifting mask:
  - Phase shifter

A.Kahng, ICCAD'03
Litho (6): Double Patterning

- Double exposure double etch
  - Double exposure double etch
  - Pitch split
- Double exposure single etch
  - Dipole decomposition (DDL)
  - Pack-unpack for contact
  - Resist freeze technology
  - Sidewall image transfer (SIT)

From Colburn, VLSI Technology 2008 Workshop

Double-Exposure Double-Etch

Starting layout

Line + cut split

Cut over line

Result:

SRAM image from K. Mistry, IEDM'07
Pitch Split Double Exposure

Starting layout

Split pattern

Overlay

With overlay misalignment

32nm Examples

Single exposure

Double exposure

IEDM'08
Litho: Design Implications

- Forbidden directions
  - Depends on illumination type
  - Poly lines in other directions can exist but need to be thicker
- Forbidden pitches
  - Nulls in the interference pattern
- Forbidden shapes in PSM
- Assist features
  - If a transistor doesn’t have a neighbor, let’s add a dummy

Litho: Current Options (Beyond 22nm)

- Immersion lithography
  - Use high index (NA ~ 1.6-1.7, \( k_1 < 0.3 \))
- Double patterning
  - NA ~ 1.2-1.35
- EUV lithography (?)
  - \( \lambda = 13.5\text{nm} \)
D. Typical 32/28nm Process

Some of the Process Features

1. Shallow-trench isolation
2. High-k/Metal-gate technology
3. Strained silicon
4. Thin-body devices (28nm, and beyond)
5. Copper interconnects with low-k dielectrics
1. Shallow Trench Isolation

- Less space needed for isolation
- Some impact on stress

![Shallow Trench Isolation Diagram]

2. Hi-k/Metal gate

- Replacement gate technology (Intel)

![Hi-k/Metal gate Diagram]

S. Natarajan, IEDM'08
K. Mistry, IEDM'07
3. Strained Silicon

- Compressive channel strain: 30% drive current increase in 90nm CMOS
- Tensile channel strain: 10% drive current increase in 90nm CMOS

Intel’s Strained Si Numbers

Performance gains:

<table>
<thead>
<tr>
<th></th>
<th>90 nm</th>
<th>65 nm</th>
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<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td><strong>μ</strong></td>
<td>20%</td>
<td>55%</td>
</tr>
<tr>
<td><strong>IDSAT</strong></td>
<td>10%</td>
<td>30%</td>
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<tr>
<td><strong>IDLIN</strong></td>
<td>10%</td>
<td>55%</td>
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S. Thompson, VLSI’06 Tutorial
**Strained Silicon**

- **No strain**
  
  \[
  W_2 \sim 2 \quad W_1 = 1
  \]

- **Strained Si**
  
  \[
  W_2 = 1.6 \quad W_1 = 1
  \]

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**5. Thin-Body Devices**

- **28nm FDSOI**

![28nm FDSOI image](image)

N. Planes, VLSI'2012

- **22nm finFET**

![22nm finFET image](image)

C. Auth, VLSI'2012
5. Interconnect

Interconnect: CMP

- **Cu interconnect: Dual damascene process**
- Ta barrier layer to prevent Cu from diffusing into Si
- Etch stop (SiN)
- Metal density rules (20%-80%)
- Slotting rules
- Also: Antenna rules
Next Lecture

› Device models