Projects

- Groups of 3
- Proposals in two weeks (2/20)
- Topics:
  - Soft errors in datapaths
  - Soft errors in memory
  - Integration of new devices into memory
  - Timing wall vs. variations, supply
  - Replica paths vs. supply and variations
  - Timing in response to variations, supply etc.
EE241 Technology

- The goal: emulate the design process and tools that industry uses by adopting a publicly available “fake” technology based on predictive models
- Two main methods to design a chip
  - "VLSI". Write RTL code that is automatically translated into standard cell gates, then place-and-routed. Focus of CS250
  - "Custom design". Analog/digital design using either individual transistors or existing standard cells. Focus of EE140/EE141
- In reality, we need both:
  - SRAM, standard cells, PLLs, etc are all custom designed, then the overall system is designed and assembled using VLSI tools

EE241 Technology--VLSI

- Synopsys 32/28nm Generic Library
  - Multi-vth Standard Cell Library with 350 cells
  - 45 IO pads
  - 35 SRAMs
  - PLL
  - Sample processors
  - Full views, hspice models, extracted parasitics
Generic Library

- **Standard Cell Datasheet**
  - CCS Modeling
  - All delay computed by VLSI tools using pre-tabulated data
  - “Characterized” at different corners, temperature, voltages for different input load and output slope
  - Also, measure leakage and dynamic power

> Synopsys

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### Conceptual VLSI “Flow”

- **Synthesis** (Synopsys Design Compiler)
- **Place-and-Route** (Synopsys IC Compiler)
- **Timing Verification** (Synopsys Primetime)
- **Simulation** (at any stage using Synopsys VCS)

**RTL**

```verilog
class always @(posedge clk)
begin
    a <= b
end
```

**Structural Verilog (no clock tree)**

```verilog
IVX4 u0 (.A(net5), .Z(net10));
```

**Structural Verilog + SPF (describing wire parasitics) + GDS (actual layout)**

```verilog
NANDX8 u1 (.A(net10), .B(net11), .Z(net30));
```
Real VLSI “Flow”

- Scripts are used to automate the configuration and running of each tool
  - In particular, Makefiles run each step only if dependency has been changed
- Place Verilog files in src/, edit Makefile/Makefrag
- One directory for each step
  - vcs-sim-rtl/ Does the RTL work?
  - dc-syn/ Synthesis (RTL to standard cells)
  - vcs-sim-gl-syn/ Do the standard cells work?
  - icc-par/ Place and route the standard cells
  - vcs-sim-gl-par/ Do the routed cells work?
  - pt-pwr/ Analyze timing and power

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EE241 Technology—Custom Design

- iPDK matches the technology used in the VLSI generic library
  - 9 layers of metal
  - Design rule manual
  - Diodes, resistors, low-voltage and high-voltage devices, multi-vth
  - PyCells for layout
  - DRC/LVS/Extraction
    - Including density check, antenna rules, etc
Conceptual Custom Design “Flow”

Schematic Entry
(Cadence Virtuoso)

Layout Entry
(Cadence Virtuoso)

DRC
(Synopsys Hercules)

LVS
(Synopsys Hercules)

Extraction
(Synopsys StarRCXT)

Simulation
(At any stage using
Synopsys HSpice)

Circuit Topology

SPICE netlist

Physical layout

Manufacturable
layout

Layout and
schematic match

SPICE netlist
including parasitic
R and C

Custom Design--Library

- The “default” devices are nmos4t and pmos4t
- Multi-vth: _hvt, _lvt
- Ios: _18, _25
- Resistors: rnpoly, rppoly (unsalicided), _wos (salicided)
- Diodes: nd, pd
- BJT: hnpn, vnpn
- Symbol name is the name in virtuoso, spice name is the device name used in netlists
Design Rule Manual

- Describes layer meanings
- Describes layout rules
  - Including density and antenna
- Provides sheet resistance estimates

Outline

- Last lecture
  - Transistor on-currents
- This lecture
  - Finish transistor modeling
Output Resistance

- Slope in I-V characteristics caused by:
  - Channel length modulation
  - Drain-induced barrier lowering (DIBL)
- Both effects increase the saturation current beyond the saturation point
- The simulations show approximately linear dependence of $I_{ds}$ on $V_{ds}$ in saturation.

[BSIM 3v3 Manual]

Output Resistance

- Channel length modulation
  - As the drain voltage increases beyond the saturation voltage $V_{dsat}$, the saturation point moves slightly closer to the source ($\Delta L$)
  - The equation is modified by replacing $L$ with $\Delta L$
  - Taylor expansion $\sqrt{I_{ds}} = I_{dsat}(1 + \frac{V_{ds}}{V_A})$

[Diagram of transistor with substrate current induced body effect]
Output Resistance

**DIBL**

- In a short channel device, source-drain distance is comparable to the depletion region widths, and the drain voltage can modulate the threshold

\[ V_{Th} = V_{Th} - \xi V_{ds} \]

- Taylor expansion

![Diagram showing short and long channel characteristics with Vds = 0.2V and Vds = 1.2V](image)

Other Models: Alpha Power Law Model

- Simple model, sometimes useful for hand analysis

\[ I_{DS} = \frac{W}{2L} \mu C_{ox} \left( V_{GS} - V_{Th} \right)^{\alpha} \]

- Parameter \( \alpha \) is between 1 and 2.

![Diagram illustrating the alpha power law model](image)

[Sakurai, Newton, JSSC 4/90]
Alpha Power Law Model

- This is not a physical model
- Simply empirical:
  - Can fit (in minimum mean squares sense) to variety of $\alpha$'s, $V_{Th}$
  - Need to find one with minimum square error – fitted $V_{Th}$ can be different from physical
  - Can also fit to $\alpha = 1$
    - What is $V_{Th}$?

$K(V_{GS} - V_{THZ})$ Model ($\alpha = 1$)

Drain current vs. gate-source voltage
## Saturation Currents

<table>
<thead>
<tr>
<th>Model</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ds} = K \frac{W}{L} (V_{GS} - V_{TH})$</td>
<td>Delay estimates with $V_{DD} \gg V_{TH}$</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \frac{\mu_C}{2} (V_{GS} - V_{TH})^2$</td>
<td>Long channel devices (rare in digital)</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \frac{\mu_C}{2} (V_{GS} - V_{TH})^\alpha$</td>
<td>Delay estimates in a wider range of $V_{DD}$'s</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \frac{\mu_C}{2} \left( (V_{GS} - V_{TH}) V_{Dsat} - \frac{V_{Dsat}^2}{2} \right)$</td>
<td>Universal model, easy to remember, does not handle stacks correctly</td>
</tr>
<tr>
<td>$I_{DS} = \frac{W}{L} \frac{\mu_C}{2} \left( \frac{E_I}{L} (V_{GS} - V_{TH}) \right)^2 \frac{E_I}{(V_{GS} - V_{TH}) + E_I L}$</td>
<td>Handles stacks correctly</td>
</tr>
</tbody>
</table>

## Transistor Leakage
Transistor Leakage

Leakage current is exponential with $V_{GS}$

$V_{DS} = 1V$

Transistor Leakage (130nm)

Two effects:
- diffusion current (like a bipolar transistor)
- exponential increase with $V_{DS}$ (DIBL)
Transistor Leakage (32nm LP PTM)

Another view of DIBL
>10x increase in leakage

Subthreshold Current

Subthreshold behavior can be modeled physically

\[ I_{ds,subth} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left( \frac{kT}{q} \right)^2 \left( \frac{V_{ds}-V_T}{m^*kT/q} \right) e^{\frac{V_{ds}-V_T}{m^*kT/q}} \left( 1 - e^{-\frac{V_{ds}}{kT}} \right) \]

\[ m = 1 + \frac{C_{ox}}{C_{ox}} \quad (m \sim 1.1-1.4) \]

Or (approx):

\[ I_{ds,subth} = I_0 \frac{W}{W_0} 10^{\left( \frac{V_{gs}-V_T}{V_{gs}} \right) - \frac{V_{gs}}{s}} \]

\[ S = 2.3m \frac{kT}{q} \]
Leakage Components

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection

Leakage ($I_{LEAK}$) Current in Amps

- weak inversion + p-n junction + DIBL + GIDL
  @ $V_D = 3.9V$
- weak inversion + p-n junction + DIBL
  @ $V_D = 2.7V$
- weak inversion + p-n junction (80 mV/dec & $V_D = 0.1V$)
- p-n junction

1. No punchthrough
2. No width effect
3. No gate leakage
Leakage Components

- **Drain-induced barrier lowering (DIBL)**
  - Voltage at the drain lowers the source potential barrier
  - Lowers $V_{TH}$, no change on $S$

- **Gate-induced drain leakage (GIDL)**
  - High field between gate and drain increases injection of carriers into substrate -> leakage
    (band-to-band leakage)
MOS Transistor as a Switch

Discharging a capacitor

• Can solve:
  \[ i_{DS} = i_{DS}(V_{DS}) \]
  \[ i_{DS} = C(V_{DS}) \frac{dV_{DS}}{dt} \]

• Prefer using equivalent resistances
• Find \( t_{pHL} \)
• Find equivalent \( C, R \)

\[ t_{pHL} = \int \frac{C(V_{DS})dV_{DS}}{i_{DS}(V_{GS},V_{DS})} \]

MOS Capacitances

Gate Capacitance

Overlap Capacitance

\[ C_{GSO} = C_{GDO} \]
\[ = C_{ox}x_dW \]
\[ = C_oW \]
(often lump fringe cap into it)
MOS Capacitances

- **Gate capacitance**
  - Non-linear channel capacitance
  - Linear overlap, fringing capacitances
  - Miller effect on overlap, fringing capacitance
- **Non-linear drain diffusion capacitance**
  - PN junction
- **Wiring capacitances**
  - Linear

Gate and Drain Capacitances

- **Gate capacitance**

- **Drain capacitance**
Gate Capacitances

- Gate capacitance is non-linear
  - First order approximation with $C_{ox}WL$ ($C_{ox}L = 1.5fF/\mu m$)
- Need to find the actual equivalent capacitance by simulating it
- Since this is a linear approximation of non-linear function, it is valid only over the certain range
  - Different capacitances for HL, LH transitions and power computation
- Drain capacitance non-linearity compensates
  - But this changes with fanout

Next Lecture

- Delay modeling